

# Semiconductors

Book S5

1985

**Field-effect transistors**

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## FIELD-EFFECT TRANSISTORS

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## DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

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- T2a** Transmitting tubes for communications, glass types
- T2b** Transmitting tubes for communications, ceramic types
- T3** Klystrons
- T4** Magnetrons for microwave heating
- T5** Cathode-ray tubes  
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6** Geiger-Müller tubes
- T7** Gas-filled tubes (will not be reprinted)
- T8** Colour display systems  
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units
- T9** Photo and electron multipliers
- T10** Plumbicon camera tubes and accessories
- T11** Microwave semiconductors and components
- T12** Vidicon and Newvicon camera tubes
- T13** Image intensifiers
- T14** Infrared detectors
- T15** Dry reed switches
- T16** Monochrome tubes and deflection units  
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

} Data collations on these subjects are available now.  
Data Handbooks will be published in 1985.

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The red series of data handbooks comprises:

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Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes ( $< 1,5\text{ W}$ ), voltage reference diodes, tuner diodes, rectifier diodes
- S2a Power diodes**
- S2b Thyristors and triacs**
- S3 Small-signal transistors**
- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Surface mounted semiconductors**
- S8 Devices for optoelectronics**  
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
- S9 Power MOS transistors**
- S10 Wideband transistors and wideband hybrid IC modules**
- S11 Microwave semiconductors**
- S12 Surface acoustic wave devices**

## INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

### EXISTING SERIES

Superseded by:

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<b>IC2</b>	<b>Bipolar ICs for video equipment</b>	<b>IC02Na and IC02Nb</b>
<b>IC3</b>	<b>ICs for digital systems in radio, audio and video equipment</b>	<b>IC01N, IC02Na and IC02Nb</b>
<b>IC4</b>	<b>Digital integrated circuits</b> CMOS HE4000B family	
<b>IC5</b>	<b>Digital integrated circuits – ECL</b> ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs	<b>IC08N</b>
<b>IC6</b>	<b>Professional analogue integrated circuits</b>	
<b>IC7</b>	<b>Signetics bipolar memories</b>	
<b>IC8</b>	<b>Signetics analogue circuits</b>	<b>IC11N</b>
<b>IC9</b>	<b>Signetics TTL logic</b>	<b>IC09N and IC15N</b>
<b>IC10</b>	<b>Signetics Integrated Fuse Logic (IFL)</b>	<b>IC13N</b>
<b>IC11</b>	<b>Microprocessors, microcomputers and peripheral circuitry</b>	

## NEW SERIES

IC01N	<b>Radio, audio and associated systems</b> Bipolar, MOS	(published 1985)
IC02Na	<b>Video and associated systems</b> Bipolar, MOS Types MAB8031AH to TDA1524A	(published 1985)
IC02Nb	<b>Video and associated systems</b> Bipolar, MOS Types TDA2501 to TEA1002	(published 1985)
IC03N	<b>Integrated circuits for telephony</b>	(published 1985)
IC04N	<b>HE4000B logic family</b> CMOS	
IC05N	<b>HE4000B logic family – uncased ICs</b> CMOS	(published 1984)
IC06N	<b>High-speed CMOS; PC54/74HC/HCT/HCU</b> Logic family	(published 1985)
IC07N	<b>High-speed CMOS; PC54/74HC/HCT/HCU – uncased ICs</b> Logic family	
IC08N	<b>ECL 10K and 100K logic families</b>	(published 1984)
IC09N	<b>TTL logic series</b>	(published 1984)
IC10N	<b>Memories</b> MOS, TTL, ECL	
IC11N	<b>Linear LSI</b>	(published 1985)
IC12N	<b>Semi-custom gate arrays &amp; cell libraries</b> ISL, ECL, CMOS	
IC13N	<b>Semi-custom</b> Integrated Fuse Logic	(published 1985)
IC14N	<b>Microprocessors, microcontrollers &amp; peripherals</b> Bipolar, MOS	
IC15N	<b>FAST TTL logic series</b>	(published 1984)

### Note

Books available in the new series are shown with their date of publication.

## COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

- C1 Programmable controller modules**  
PLC modules, PC20 modules
- C2 Television tuners, coaxial aerial input assemblies, surface acoustic wave filters**
- C3 Loudspeakers**
- C4 Ferroxcube potcores, square cores and cross cores**
- C5 Ferroxcube for power, audio/video and accelerators**
- C6 Synchronous motors and gearboxes**
- C7 Variable capacitors**
- C8 Variable mains transformers**
- C9 Piezoelectric quartz devices**
- C10 Connectors**
- C11 Non-linear resistors**  
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
- C12 Potentiometers, encoders and switches**
- C13 Fixed resistors**
- C14 Electrolytic and solid capacitors**
- C15 Ceramic capacitors**
- C16 Permanent magnet materials**
- C17 Stepping motors and associated electronics**
- C18 Direct current motors**
- C19 Piezoelectric ceramics**
- C20 Wire-wound components for TVs and monitors**
- C21\* Assemblies for industrial use**  
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices
- C22 Film capacitors**

\* Will be issued in 1985.

## SELECTION GUIDE





## N-channel junction field-effect transistors

type number	envelope		RATINGS		CHARACTERISTICS						remarks	page
	$\pm V_{DS}$	$P_{tot}$ at $T_{amb}$	$V$	$mW$	$\pm V(p)GS$ max.	$ I_{DSS}$ min.-max.	$-I_{GSS}$ max.	$ y_{fs} $ min. $f = 1$ kHz	$C_{rs}$ typ.	$F$ typ.		
			$^{\circ}C$	$nA$	$V$	$mA$	$mS$	$pF$	$dB$			
BC264A						2,0-4,5	2,5				hi-fi amplifiers and a.f. equipment	51
BC264B						3,5-6,5	3,0					51
BC264C		300	25	10	> 0,5	5,0-8,0	3,5	1,2	0,5			51
BC264D						7,0-12,0	4,0					51
BF245A						2,0-6,5	3,0-6,5	1,1	1,5		d.c., l.f. and h.f. amp.	57
BF245B		300	75	5	8,0	6-15						57
BF245C						12-25						57
BF247A						30-80						69
BF247B		250	75	5	0,6-14,5	60-140	8	3,5	-		v.h.f. and u.h.f. amp. general purpose sw.	69
BF247C						110-250						69
BF256A						3-7						71
BF256B		300	75	5	-	6-13	4,5	0,7	7,5		v.h.f. and u.h.f. appl.	71
BF256C						11-18						71
BF410A						0,7-3,0	2,5				r.f. stages f.m. portables	83
BF410B						2,5-7,0	4,0				r.f. stages car radios	83
BF410C		300	75	10	typ. 1,5	6-12	6,0	0,3	1,5		r.f. stages mains radios	83
BF410D		20*			typ. 2,2	10-18	7,0				mixer stages	83
BF510						0,7-3,0	2,5				r.f. stages f.m. portables	87
BF511		250	65	10	typ. 0,8	2,5-7,0	4,0	0,3	1,5		r.f. stages car radios	87
BF512					typ. 1,5	6-12	6,0				r.f. stages mains radios	87
BF513					typ. 2,2	10-18	7,0				mixer stages	87
BFR30		25	65	0,2	5	4-10	1,0-4,0	< 1,5	-		low-level general purpose amplifiers	101
BFR31						1-5	1,5-4,5					101
BFR101A		30	60	5	1,0	0,2-1,5	1,2	-	-		source follower	111
BFR101B						1-5	2,5					111

\* Asymmetrical.

N-channel junction field-effect transistors

type number	envelope	RATINGS		CHARACTERISTICS							remarks	page
		$\pm V_{DS}$ V	$P_{tot}$ at $T_{amb}$ mW oC	$-I_{GSS}$ max. nA	$I_{DSS}$ min.-max. mA	$-V(P)GS$ max. V	$ V_{fs} $ min. f = 1 kHz mS	$C_{rs}$ typ. pF	F typ. dB			
BFT46	SOT-23	25	250 65	0,2	0,2-1,5	1,2	1,0	< 1,5	-	general purpose ampl.	119	
BFW10	TO-72	30	300 25	0,1	8-20 4-10	8 6	3,5-6,5 3,0-6,5	0,6	< 2,5	broad band up to 300 MHz and differential ampl.	127 127	
BFW12	TO-72	30	150 110	0,1	1-5 0,2-1,5	2,5 1,2	2,0 1,0	< 0,8	-	low current-low voltage applications	139 139	
BFW61	TO-72	25	300 25	1,0	2-20	8	2,0-6,5	< 2,0	-	general purpose ampl.	149	
2N3822	TO-72	50	300 25	0,1	2-10	6	3,0-6,5	< 3,0	< 5	general purpose h.f. ampl.	167	
2N3823	TO-72	30	300 25	0,5	4-20	8	3,5-6,5	< 2,0	< 2,5	industrial i.f./r.f. ampl.	169	

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS			CHARACTERISTICS						page	
		$\pm V_{DS}$ V	$P_{tot}$ at $T_{amb}$ mW	$\theta_C$ $^{\circ}C$	$-I_{GSS}$ ( $I_{SGO}$ ) max. pA	$I_{DSS}$ min. mA	$-V_{PIGS}$ max. V	$r_{ds\ on}$ max. $\Omega$	$C_{rs}$ max. pF	$t_{on}$ max. ns		$t_{off}$ max. ns
BSR56					50	10	25			9	25	151
BSR57	SOT-23	40	250	65	20	6	40	5		10	50	151
BSR58					8	4	60			20	100	151
BSV78					50	11	25	5		10	10	155
BSV79	TO-18	40	350	25	20	7,0	40	5		18	16	155
BSV80					10	5,0	60			30	32	155
PBMF4391		40			50	10	30	3,5		5	15	163
PBMF4392	SOT-23	40	250	65	25	5	60	3,5		5	15	163
PBMF4393		40			5	3	100	3,5		5	15	163
2N3966	TO-72	30	300	25	2	6	220	1,5		120	100	171
2N4091					30	10	30			25	40	175
2N4092	TO-18	40	1800	25	15	7,0	50	5		35	60	175
2N4093					8	5,0	80			60	80	175
2N4391					50	10	30			20	20	179
2N4392	TO-18	40	1800	25	25	5,0	60	3,5		15	35	179
2N4393					5	3,0	100			50	50	179
2N4856		40			50	10	25			9	25	183
2N4857		40			20	6	40			10	50	183
2N4858		40			8	4	60		8	20	100	183
2N4859	TO-18	30	360	25	50	10	25			9	25	183
2N4860		30			20	6	40			10	50	183
2N4861		30			8	4	60			20	100	183

N-channel junction field-effect transistors for differential amplifiers

type	RATINGS				CHARACTERISTICS								
	individual transistor		total device		individual transistor			total device					
	$\pm V_{DS}$	$P_{tot}$ at $T_{amb}$ mW	$P_{tot}$ at $T_{amb}$ mW	$P_{tot}$ at $T_{amb}$ °C	$-I_{GSS}$ max. pA	$ DSS $ mA	$-V(P)GS$ max. V	$ \Delta V_{GS} $ max. mV	$\left  \frac{d\Delta V_{GS}}{dT} \right $ max. $\mu V/K$	$\left  \Delta \frac{1}{g_{fs}} \right $ max. $\Omega$	$\left  \Delta \frac{g_{os}}{g_{fs}} \right $ max. $\mu V/V$	CMRR min. dB	page
BFO10								5	5	6	10	100	93
BFO11								10	5	6	30	90	93
BFO12								10	10	12	30	90	93
BFO13			250	75		100	3.5	10	20	12	30	90	93
BFO14	30	250	75	75		0.5-10		15	20	12	30	90	93
BFO15								20	20	20	30	90	93
BFO16								50	40	30	100	80	93
BFS21		300	25	30		> 1	6	20	75	15	1000	60	113
BFS21A				100				10	40	7.5	500	66	113

## Dual-gate N-channel MOS-FETs

type number	envelope	RATINGS		CHARACTERISTICS						remarks	page
		V <sub>DS</sub>	P <sub>rot</sub> at T <sub>amb</sub>	± I <sub>G1-SS</sub> ± I <sub>G2-SS</sub> max.	I <sub>DSS</sub>	-V <sub>(P)GS</sub> -V <sub>(P)G1-S</sub>	V <sub>fs</sub>   f = 1 kHz min.	C <sub>rs</sub> typ.	F max.		
	V	mW	°C	nA	mA	V	mS	ff	dB		
BF960*	SOT-103	20	225	50	2-20	< 3,5	9,5	25	2,8**	r.f. stage — UHF TV tuner	189
BF964*	SOT-103	20	225	50	2-20	< 2,5	15	25	2,8	r.f./mixer stage VHF TV tuner	193
BF966*	SOT-103	20	225	50	2-20	< 2,5	15	25	3,9	r.f. stage UHF TV tuner	197
BF980*	SOT-103	18	225	25	—	< 1,3	17	25	2,8**	r.f./mixer stage VHF TV tuner	201
BF981*	SOT-103	20	225	50	4-25	< 2,5	10	20	2,0	r.f./mixer stage VHF TV tuner	205
BF982*	SOT-103	20	225	25	—	< 1,3	20	30	1,2**	r.f./mixer stage VHT TV tuner and FM radio tuner	213
BF989*	SOT-143	20	200	50	2-20	< 2,7	9,5	25	2,8**	u.h.f. — r.f. stage	217
BF990*	SOT-143	18	200	25	—	< 1,3	17	25	2,8**	u.h.f. — r.f. stage	219
BF991*	SOT-143	20	200	50	4-25	< 2,5	10	20	2,0	v.h.f. — r.f. stage	223
BF992*	SOT-143	20	200	25	—	< 1,3	20	30	1,2**	v.h.f. — r.f. stage	225
BF994*	SOT-143	20	200	50	2-20	< 2,5	15	25	2,8	v.h.f. — r.f. stage	227
BF996*	SOT-143	20	200	50	2-20	< 2,5	15	25	3,9	u.h.f. — r.f. stage	231
BF984*	TO-72	20	300	10	20-55	1,5-3,8	12	30	3,0	general industrial	243

\* Protected against excessive input voltage surges.

\*\* Typical.

N-channel MOS-FETs for switching

type number	envelope	RATINGS			CHARACTERISTICS				page
		V <sub>DB</sub> V <sub>SB</sub> V	P <sub>tot</sub> at T <sub>amb</sub> mW	oC	± I <sub>GSS</sub> max. nA	r <sub>ds on</sub> max. Ω	C <sub>r</sub> s max. pF	t <sub>on</sub> /t <sub>off</sub> max. ns	
BFR29	TO-72	30	200	25	0,01	—	0,7	—	235
BSD10	TO-72	15	275	25	—	30	0,6	1/5	253
BSD12		25							
BSD20	SOT-143	15	230	25	—	30	0,6	1/5	257
BSD22		25							
BSD212	TO-72	15	275	25	—	70	0,6	1/5	261
BSD213		15							
BSD214		25							
BSD215		25							
BSS83	SOT-143	15	230	25	—	45	0,6	1/5	265
BSV81	TO-72	30	200	25	0,01	100	0,5	—	329

P-channel vertical D-MOSFETs for switching

type number	envelope	RATINGS			CHARACTERISTICS				page		
		V <sub>DS</sub> V	I <sub>D</sub> mA	P <sub>tot</sub> at T <sub>amb</sub> mW	oC	V <sub>GS</sub> (th) V	R <sub>DSon</sub> typ. Ω	max. Ω		Y <sub>fs</sub> typ. mS	t <sub>on</sub> /t <sub>off</sub> max. ns
BST100	TO-92 var.	60	300	1000	25	1,5-3,5	4,5	6	200	4/20	313
BST110	TO-92 var.	50	300	830	25	1,5-3,5	7,5	10	125	4/20	317
BST120	SOT-89	60	300	1000	25	1,5-3,5	4,5	6	200	4/20	321
BST122	SOT-89	50	250	1000	25	1,5-3,5	7,5	10	125	4/20	325

## N-channel vertical D-MOSFETs for switching

type number	envelope	RATINGS				CHARACTERISTICS					
		V <sub>DS</sub>	I <sub>D</sub>	P <sub>tot</sub> at T <sub>amb</sub>	V <sub>GS(th)</sub>	R <sub>DSon</sub>	Y <sub>fs</sub>	t <sub>on</sub> /t <sub>off</sub>	page		
		V	mA	mW °C	V	typ. Ω	max. Ω	typ. mS		max. ns	
BS107	TO-92 var.	200	120	500	25	1,8 (typ.)	15	28	200	10/10	249
BS170	TO-92 var.	60	500	830	25	0,8-3,0	2,5	5	200	10/10	251
BS170A	TO-92 var.	80	500	1000	25	1,5-3,5	2	4	300	10/15	269
BS172A	TO-92 var.	80	300	830	25	1,5-3,5	7	10	150	10/10	273
BS174A	TO-92 var.	200	300	1000	25	0,8-2,8	6	12	250	10/25	277
BS176A	TO-92 var.	180	300	1000	25	0,7-2,7	7	10	250	10/15	281
BS178	TO-126	450	750	15000	75	2,0-4,0	10	14	400	10/100	285
BS180	SOT-89	80	500	1000	25	1,5-3,5	2	4	300	10/15	289
BS182	SOT-23	80	175	300	25	1,5-3,5	7	10	150	10/10	293
BS184	SOT-89	200	250	1000	25	0,8-2,8	6	12	250	10/25	297
BS186	SOT-89	180	300	1000	25	0,7-2,7	7	10	250	10/15	301
BS190	TO-39	80	500	2500	25*	1,5-3,5	2	4	300	10/15	305
BS197	TO-18	180	300	1500	25*	0,7-2,7	7	10	250	10/15	309
2N6659	TO-39	35	1400	6250	25*	0,8-2,0	1,5	5	170	10/20	335
2N6660	TO-39	60	1100	6250	25*	0,8-2,0	1,8	5	170	10/20	335
2N6661	TO-39	90	900	6250	25*	0,8-2,0	2,4	5,3	170	10/20	335

\* T<sub>c</sub>.





TYPE NUMBER SURVEY



In this alphanumeric list we present all n-channel field-effect transistors mentioned in this handbook.

type number	envelope	$\pm V_{DS}$ max. V	$I_{DSS}$ mA	application	page
BC264A	TO-92 var.	30	2,0 - 4,5	hi-fi amplifiers and a.f. equipment	51
BC264B			3,5 - 6,5		51
BC264C			5,0 - 8,0		51
BC264D			7,0 - 12,0		51
BF245A	TO-92 var.	30	2,0 - 6,5	d.c., l.f. and h.f. amplifiers	57
BF245B			6,0 - 15,0		57
BF245C			12 - 25		57
BF247A	TO-92 var.	25	30 - 80	v.h.f. and u.h.f. ampl. general purpose switch	69
BF247B			60 - 140		69
BF247C			110 - 250		69
BF256A	TO-92 var.	30	3 - 7	v.h.f. and u.h.f.	71
BF256B			6 - 13		71
BF256C			11 - 18		71
BF410A	TO-92 var.	20*	0,7 - 3,0	r.f. stages f.m. portables r.f. stages car radios r.f. stages mains radios mixer stages	83
BF410B			2,5 - 7,0		83
BF410C			6 - 12		83
BF410D			10 - 18		83
BF510	SOT-23	20	0,7 - 3,0	r.f. stage f.m. portables r.f. stage car radios r.f. stage mains radios mixer stages	87
BF511			2,5 - 7,0		87
BF512			6 - 12		87
BF513			10 - 18		87
BF960	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	189
BF964	SOT-103	20	2 - 20	r.f./mixer stage VHF TV tuner	193
BF966	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	197
BF980	SOT-103	18	—	r.f. stage UHF TV tuner	201
BF981	SOT-103	20	4 - 25	r.f./mixer stage VHF TV tuner	205
BF982	SOT-103	20	—	r.f./mixer stage VHF TV tuner and FM radio tuner	213
BF989	SOT-143	20	2 - 20	u.h.f. TV tuners	217
BF990	SOT-143	18	—	u.h.f. TV tuners	219
BF991	SOT-143	20	4 - 25	v.h.f. TV and f.m. tuners	223
BF992	SOT-143	20	—	v.h.f. TV and f.m. tuners	225
BF994	SOT-143	20	2 - 20	u.h.f./v.h.f. TV tuners	227
BF996	SOT-143	20	2 - 20	u.h.f. TV tuners	231
BFQ10	TO-71	30	0,5 - 10	low level differential amplifiers	93
BFQ11					93
BFQ12					93
BFQ13					93
BFQ14					93
BFQ15					93
BFQ16	TO-72	30**	10 - 40	v.h.f./low leakage/low noise	93
BFR29					235

\* Asymmetrical.

\*\*  $V_{DB}$ .

# TYPE NUMBER SURVEY

type number	envelope	$\pm V_{DS}$ max. V	$I_{DSS}$ mA	application	page
BFR30	SOT-23	25	4 - 10	general purpose amplifiers	101
BFR31			1 - 5		101
BFR84	TO-72	20	20 - 55	general industrial	243
BFR101A	SOT-143	30	0,2 - 1,5	source follower	111
BFR101B			1,0 - 5,0		111
BFS21	SOT-52	30	> 1	low level differential amplifiers	113
BFS21A					113
BFT46	SOT-23	25	0,2 - 1,5	general purpose amplifiers	119
BFW10	TO-72	30	8 - 20	wide-band up to 300 MHz and differential amplifiers	127
BFW11			4 - 10		127
BFW12	TO-72	30	1 - 5	low current-low voltage	139
BFW13			0,2 - 1,5		139
BFW61	TO-72	25	2 - 20	general purpose	149
BS107	TO-92 var.	200	< 0,03	relay and line-transformer drivers	249
BS170	TO-92 var.	60	< 0,5 $\mu$ A		251
BSD10	TO-72	10	—	switch/convertor/chopper	253
BSD12		20	253		
BSD20	SOT-143	10	—	switch/convertor/chopper	257
BSD22		20	257		
BSD212	TO-72	10	—	switch/convertor/chopper	261
BSD213		10	—		261
BSD214		20	—		261
BSD215		20	—		261
BSR56		SOT-23	40		> 50
BSR57	20 - 100			151	
BSR58	8 - 80			151	
BSS83	SOT-143	10	—	switch/switch driver	265
BST70A	TO-92 var.	80	0,5	} relay, high-speed and line-transformer drivers	269
BST72A	TO-92 var.	80	0,3		273
BST74A	TO-92 var.	200	0,3		277
BST76A	TO-92 var.	180	0,3		281
BST78	TO-202	450	0,75		285
BST80	SOT-89	80	0,5*		289
BST82	SOT-23	80	0,175*		293
BST84	SOT-89	200	0,25*	297	
BST86	SOT-89	180	0,3*	301	

\*  $I_{Dmax}$  (A).

# TYPE NUMBER SURVEY

type number	envelope	$\pm V_{DS}$ max. V	$I_{DSS}$ mA	application	page
BST90	TO-39	80	0,5		305
BST97	TO-18	180	0,3		309
BST100	TO-92 var.	60	0,3	relay, high-speed and	313
BST110	TO-92 var.	50	0,25	line-transformer drivers	317
BST120	SOT-89	60	0,3		321
BST122	SOT-89	50	0,25		325
BSV78			> 50		155
BSV79	TO-18	40	> 20	switch	155
BSV80			> 10		155
BSV81	TO-72	30*	—	switch/chopper	329
PBMF4391			> 40		163
PBMF4392	SOT-123	40	> 25	switch/chopper	163
PBMF4393			> 5		163
2N3822	TO-72	50	2-10	general purpose h.f. ampl.	167
2N3823	TO-72	30	4-20	industrial i.f./r.f. ampl.	169
2N3966	TO-72	30	> 2	low power switch	171
2N4091			> 30		175
2N4092	TO-18	40	> 15	low power switch	175
2N4093			> 8		175
2N4391			> 50		179
2N4392	TO-18	40	> 25	low power switch/chopper	179
2N4393			> 5		179
2N4856		40	> 50		183
2N4857		40	> 20		183
2N4858		40	> 8		183
2N4859	TO-18	30	> 50	low power switch/chopper	183
2N4860		30	> 20		183
2N4861		30	> 8		183
2N6659		35	1,4*		335
2N6660	TO-39	60	1,1*	H.F. inverters and line drivers	335
2N6661		90	0,9*		335

\*  $I_{Dmax}$  (A).



## GENERAL

**Type designation**

**Rating systems**

**Letter symbols**

**s-parameters**

**TO-92 variant transistors on tape**

**Tape and reel specification for**

**SOT-23 and SOT-143**

**Soldering recommendations for**

**SOT-23, SOT-143 and SOT-89**

**Soldering recommendations for**

**SOT-37 and SOT-103**

**Thermal characteristics for**

**SOT-23 and SOT-143**





## PRO ELECTRON TYPE DESIGNATION CODE FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices — as opposed to integrated circuits —, multiples of such devices and semiconductor chips.

“Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do.”

A basic type number consists of:

*TWO LETTERS FOLLOWED BY A SERIAL NUMBER*

### FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

- A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
- B. SILICON or other material with band gap of 1,0 to 1,3 eV.
- C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
- R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

### SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

- A. DIODE; signal, low power
- B. DIODE; variable capacitance
- C. TRANSISTOR; low power, audio frequency ( $R_{th\ j-mb} > 15\ K/W$ )
- D. TRANSISTOR; power, audio frequency ( $R_{th\ j-mb} \leq 15\ K/W$ )
- E. DIODE; tunnel
- F. TRANSISTOR; low power, high frequency ( $R_{th\ j-mb} > 15\ K/W$ )
- G. MULTIPLE OF DISSIMILAR DEVICES — MISCELLANEOUS; e.g. oscillator
- H. DIODE; magnetic sensitive
- L. TRANSISTOR; power, high frequency ( $R_{th\ j-mb} \leq 15\ K/W$ )
- N. PHOTO-COUPLER
- P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
- Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
- R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ( $R_{th\ j-mb} > 15\ K/W$ )
- S. TRANSISTOR; low power, switching ( $R_{th\ j-mb} > 15\ K/W$ )
- T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ( $R_{th\ j-mb} \leq 15\ K/W$ )
- U. TRANSISTOR; power, switching ( $R_{th\ j-mb} \leq 15\ K/W$ )
- X. DIODE: multiplier, e.g. varactor, step recovery
- Y. DIODE; rectifying, booster
- Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

# TYPE DESIGNATION

## SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.\*  
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.\*

This letter has no fixed meaning except W, which is used for transient suppressor diodes.

## VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

## SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

### 1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*

The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage

- A. 1% (according to IEC 63: series E96)
- B. 2% (according to IEC 63: series E48)
- C. 5% (according to IEC 63: series E24)
- D. 10% (according to IEC 63: series E12)
- E. 20% (according to IEC 63: series E6)

The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.

The letter 'V' is used instead of the decimal point.

### 2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*

The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage  $V_R$ . The letter 'V' is used as above.

### 3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*

The NUMBER indicates the rated maximum repetitive peak reverse voltage ( $V_{RRM}$ ) or the rated repetitive peak off-state voltage ( $V_{DRM}$ ), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

### 4. RADIATION DETECTORS: *ONE NUMBER*, preceded by a hyphen (-)

The NUMBER indicates the depletion layer in  $\mu\text{m}$ . The resolution is indicated by a version LETTER.

### 5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER*, preceded by a stroke (/).

The NUMBER indicates how many basic devices are assembled into the array.

\* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

## RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

### DEFINITIONS OF TERMS USED

*Electronic device.* An electronic tube or valve, transistor or other semiconductor device.

#### Note

This definition excludes inductors, capacitors, resistors and similar components.

*Characteristic.* A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

*Bogey electronic device.* An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

*Rating.* A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

#### Note

Limiting conditions may be either maxima or minima.

*Rating system.* The set of principles upon which ratings are established and which determine their interpretation.

#### Note

The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

### ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

## DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

## DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

# LETTER SYMBOLS FOR TRANSISTORS AND SIGNAL DIODES

based on IEC Publication 148

## LETTER SYMBOLS FOR CURRENTS, VOLTAGES AND POWERS

### Basic letters

The basic letters to be used are:

I, i = current  
V, v = voltage  
P, p = power.

Lower-case basic letters shall be used for the representation of instantaneous values which vary with time.

In all other instances upper-case basic letters shall be used.

### Subscripts

A, a	Anode terminal
(AV), (av)	Average value
B, b	Base terminal, for MOS devices: Substrate
(BR)	Breakdown
C, c	Collector terminal
D, d	Drain terminal
E, e	Emitter terminal
F, f	Forward
G, g	Gate terminal
K, k	Cathode terminal
M, m	Peak value
O, o	As third subscript: The terminal not mentioned is open circuited
R, r	As first subscript: Reverse. As second subscript: Repetitive. As third subscript: With a specified resistance between the terminal not mentioned and the reference terminal.
(RMS), (rms)	R. M. S. value
S, s	{ As first or second subscript: Source terminal (for FETS only) As second subscript: Non-repetitive (not for FETS) As third subscript: Short circuit between the terminal not mentioned and the reference terminal
X, x	Specified circuit
Z, z	Replaces R to indicate the actual working voltage, current or power of voltage reference and voltage regulator diodes.

Note: No additional subscript is used for d. c. values.

Upper-case subscripts shall be used for the indication of:

- a) continuous (d. c.) values (without signal)  
Example  $I_B$
- b) instantaneous total values  
Example  $i_B$
- c) average total values  
Example  $I_{B(AV)}$
- d) peak total values  
Example  $I_{BM}$
- e) root-mean-square total values  
Example  $I_{B(RMS)}$

Lower-case subscripts shall be used for the indication of values applying to the varying component alone:

- a) instantaneous values  
Example  $i_b$
- b) root-mean-square values  
Example  $I_{b(rms)}$
- c) peak values  
Example  $I_{bm}$
- d) average values  
Example  $I_{b(av)}$

Note: If more than one subscript is used, subscript for which both styles exist shall either be all upper-case or all lower-case.

#### **Additional rules for subscripts**

##### Subscripts for currents

**Transistors:** If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples:  $I_B$ ,  $i_B$ ,  $i_b$ ,  $I_{bm}$

**Diodes:** To indicate a forward current (conventional current flow into the anode terminal) the subscript F or f should be used; for a reverse current (conventional current flow out of the anode terminal) the subscript R or r should be used.

Examples:  $I_F$ ,  $I_R$ ,  $i_F$ ,  $I_{f(rms)}$

Subscripts for voltages

Transistors: If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples:  $V_{BE}$ ,  $v_{BE}$ ,  $v_{be}$ ,  $V_{bem}$

Diodes: To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used; for a reverse voltage (anode negative with respect to cathode) the subscript R or r should be used.

Examples:  $V_F$ ,  $V_R$ ,  $v_F$ ,  $V_{rm}$

Subscripts for supply voltages or supply currents

Supply voltages or supply currents shall be indicated by repeating the appropriate terminal subscript.

Examples:  $V_{CC}$ ,  $I_{EE}$

Note: If it is necessary to indicate a reference terminal, this should be done by a third subscript

Example:  $V_{CCE}$

Subscripts for devices having more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal followed by a number; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples:  $I_{B2}$  = continuous (d. c.) current flowing into the second base terminal

$V_{B2-E}$  = continuous (d. c.) voltage between the terminals of second base and emitter

Subscripts for multiple devices

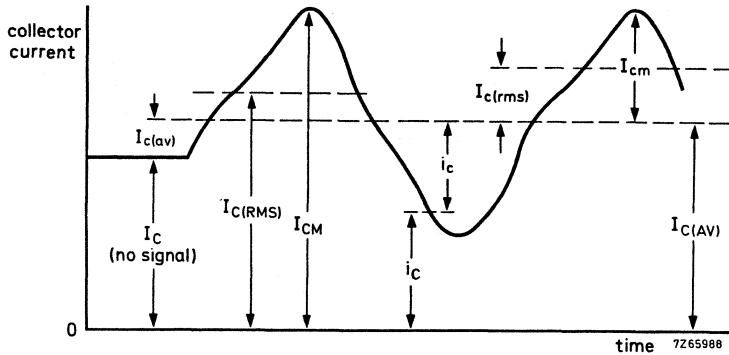
For multiple unit devices, the subscripts are modified by a number preceding the letter subscript; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples:  $I_{2C}$  = continuous (d. c.) current flowing into the collector terminal of the second unit

$V_{1C-2C}$  = continuous (d. c.) voltage between the collector terminals of the first and the second unit.

### Application of the rules

The figure below represents a transistor collector current as a function of time. It consists of a continuous (d.c.) current and a varying component.



### LETTER SYMBOLS FOR ELECTRICAL PARAMETERS

#### Definition

For the purpose of this Publication, the term "electrical parameter" applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

#### Basic letters

The following is a list of the most important basic letters used for electrical parameters of semiconductor devices.

- B, b = susceptance; imaginary part of an admittance
- C = capacitance
- G, g = conductance; real part of an admittance
- H, h = hybrid parameter
- L = inductance
- R, r = resistance; real part of an impedance
- X, x = reactance; imaginary part of an impedance
- Y, y = admittance;
- Z, z = impedance;



Upper-case letters shall be used for the representation of:

- a) electrical parameters of external circuits and of circuits in which the device forms only a part;
- b) all inductances and capacitances.

Lower-case letters shall be used for the representation of electrical parameters inherent in the device (with the exception of inductances and capacitances).

### Subscripts

#### General subscripts

The following is a list of the most important general subscripts used for electrical parameters of semiconductor devices:

F, f	= forward; forward transfer
I, i (or 1)	= input
L, l	= load
O, o (or 2)	= output
R, r	= reverse; reverse transfer
S, s	= source

Examples:  $Z_S$ ,  $h_f$ ,  $h_F$

The upper-case variant of a subscript shall be used for the designation of static (d.c.) values.

Examples:  $h_{FE}$  = static value of forward current transfer ratio in common-emitter configuration (d.c. current gain)

$R_E$  = d.c. value of the external emitter resistance.

Note: The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript shall be used for the designation of small-signal values.

Examples:  $h_{fe}$  = small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration

$Z_e = R_e + jX_e$  = small-signal value of the external impedance

Note: If more than one subscript is used, subscripts for which both styles exist shall either be all upper-case or all lower-case

Examples:  $h_{FE}$ ,  $y_{RE}$ ,  $h_{fe}$

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer

Examples:  $h_i$  (or  $h_{11}$ )  
 $h_o$  (or  $h_{22}$ )  
 $h_f$  (or  $h_{21}$ )  
 $h_r$  (or  $h_{12}$ )

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples:  $h_{fe}$  (or  $h_{21e}$ ),  $h_{FE}$  (or  $h_{21E}$ )

**Distinction between real and imaginary parts**

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

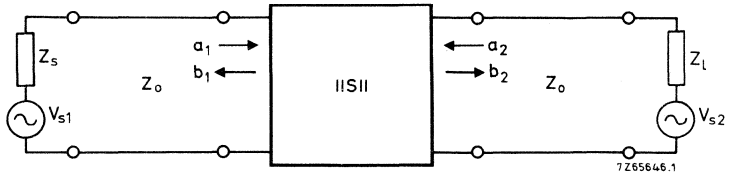
Examples:  $Z_i = R_i + jX_i$   
 $y_{fe} = g_{fe} + jb_{fe}$

If such symbols do not exist or if they are not suitable, the following notation shall be used:

Examples:  $\text{Re}(h_{ib})$  etc. for the real part of  $h_{ib}$   
 $\text{Im}(h_{ib})$  etc. for the imaginary part of  $h_{ib}$

## SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to traveling wave conditions. The figure below shows a two-port network with the incident and reflected waves  $a_1$ ,  $b_1$ ,  $a_2$  and  $b_2$ .



$$a_1 = \frac{V_{i1}}{\sqrt{Z_0}}$$

$$a_2 = \frac{V_{i2}}{\sqrt{Z_0}}$$

1)

$$b_1 = \frac{V_{r1}}{\sqrt{Z_0}}$$

$$b_2 = \frac{V_{r2}}{\sqrt{Z_0}}$$

$Z_0$  = characteristic impedance of the transmission line in which the two-port is connected.

$V_i$  = incident voltage

$V_r$  = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \left. \frac{b_1}{a_1} \right|_{a_2 = 0}$$

$$s_r = s_{12} = \left. \frac{b_1}{a_2} \right|_{a_1 = 0}$$

$$s_f = s_{21} = \left. \frac{b_2}{a_1} \right|_{a_2 = 0}$$

$$s_o = s_{22} = \left. \frac{b_2}{a_2} \right|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$  = Input reflection coefficient.

The complex ratio of the reflected wave and the incident wave at the input, under the conditions  $Z_1 = Z_0$  and  $V_{s2} = 0$ .

$s_r = s_{12}$  = Reverse transmission coefficient.

The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions  $Z_s = Z_0$  and  $V_{s1} = 0$ .

$s_f = s_{21}$  = Forward transmission coefficient.

The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions  $Z_1 = Z_0$  and  $V_{s2} = 0$ .

$s_o = s_{22}$  = Output reflection coefficient.

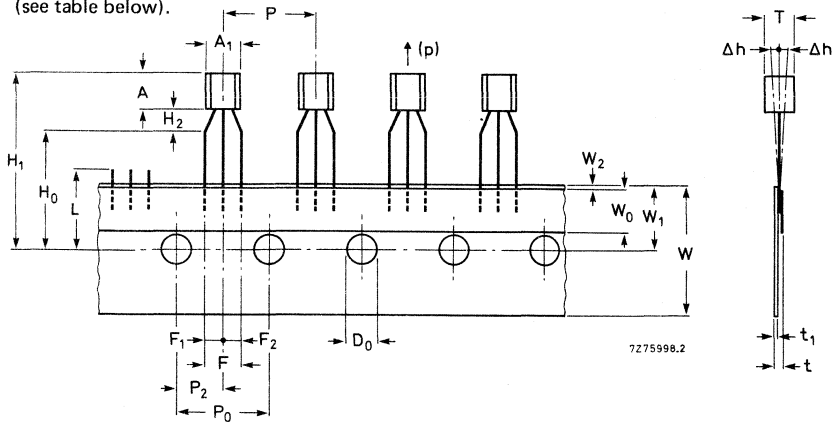
The complex ratio of the reflected wave and the incident wave at the output, under the conditions  $Z_s = Z_0$  and  $V_{s1} = 0$ .

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Fig. 1 (see table below).

Dimensions in mm



Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A <sub>1</sub>	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P <sub>0</sub>		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P <sub>2</sub>		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		+ 0,6 - 0,2	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W <sub>0</sub>		6		± 0,2	
Hole position	W <sub>1</sub>		9		+ 0,7 - 0,5	
Hold-down tape position	W <sub>2</sub>		0,5		± 0,2	
Lead wire clinch height	H <sub>0</sub>		16		± 0,5	
Component height	H <sub>1</sub>			32,25		
Length of snapped leads	L			11,0		
Feed hole diameter	D <sub>0</sub>		4		± 0,2	
Total tape thickness	t			1,2		t <sub>1</sub> 0,3-0,6
Lead-to-lead distance	F <sub>1</sub> , F <sub>2</sub>		2,54		+ 0,4 - 0,1	
Clinch height	H <sub>2</sub>			3		
Pull-out force	(p)	6N				

# TAPE

## PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000\*.

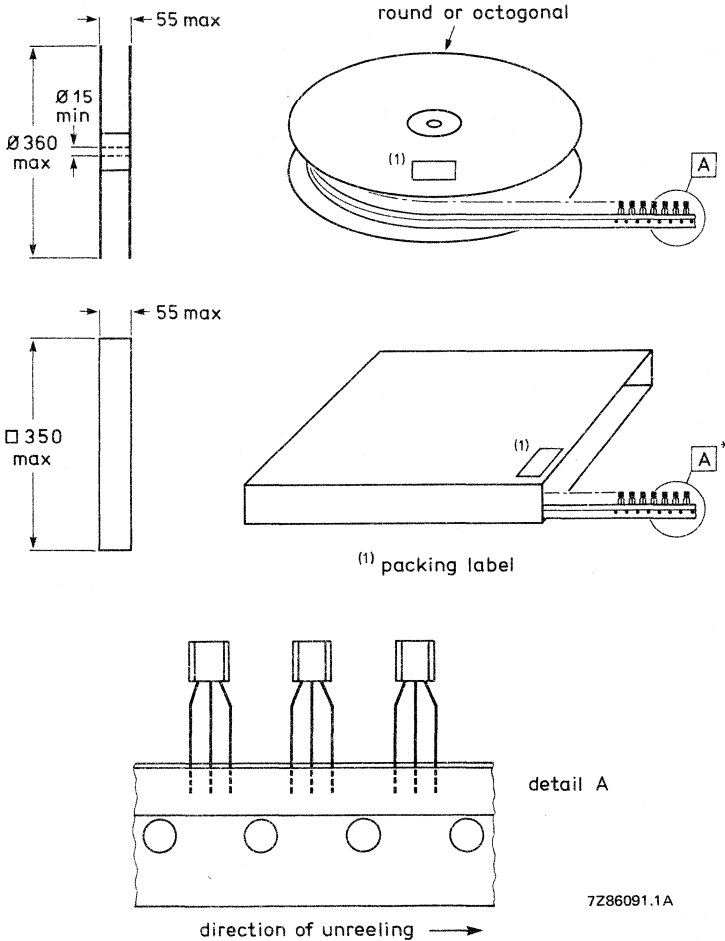


Fig. 2 Dimensions (in mm) of reel and box.

## DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

**TAPE SPLICING**

Slice the carrier tape on the back and/or front so that the feed hole pitch ( $P_0$ ) is maintained (see Fig. 3).

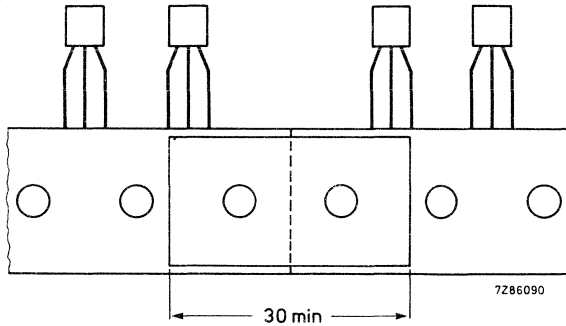


Fig. 3 Jointing tape with splicing patch.

- \* The ammobox has 80 layers of 25 transistors each.  
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.  
The ammobox is accessible from both sides enabling the user to choose between "normal" (see Fig. 2) and "reverse" tape.

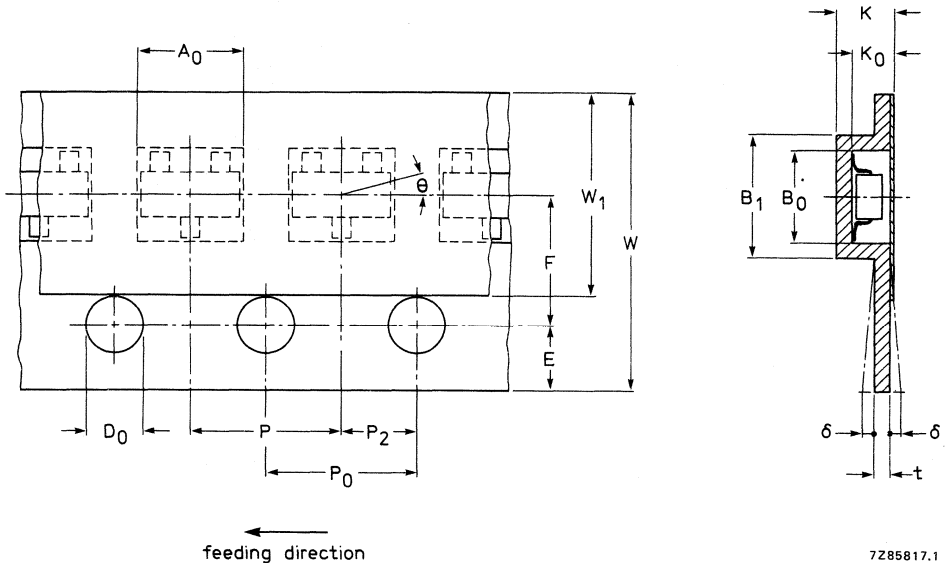




## TAPE AND REEL SPECIFICATION

Semiconductors in SOT-23 and SOT-143 encapsulations can be delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.

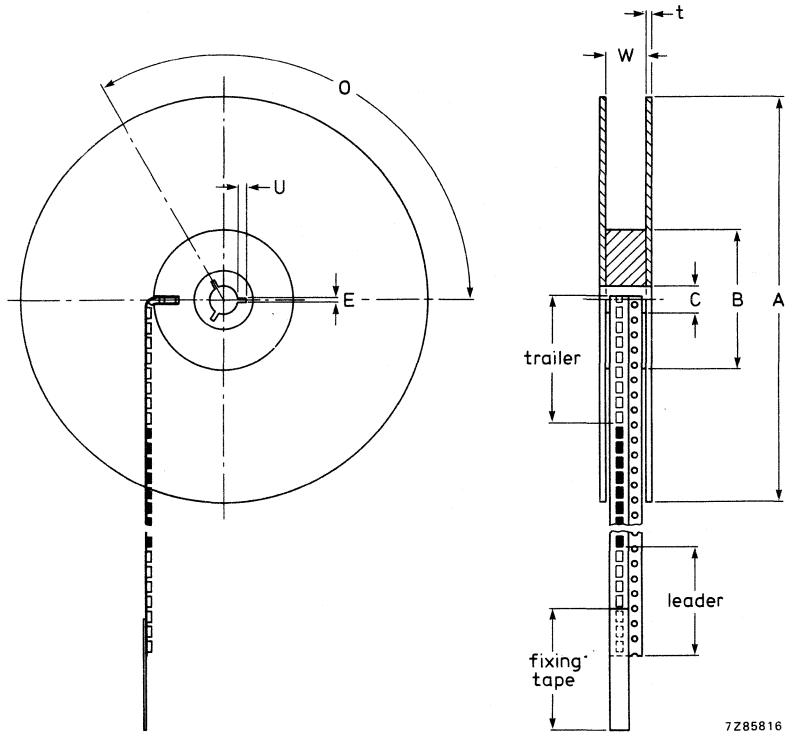
A separate cross-section for SOD-80 encapsulation is given in Fig. 3.



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Fig. 1 Configuration of bandolier. Dimensions in mm.

Compartment			Centre line dimensions		
		tol.			tol.
length	$A_0$ component length	+0,2	length direction	$P_2$	2,0 ±0,05
width	$B_0$ component width	+0,2	width direction	$F$	3,5 ±0,05
depth	$K_0$	0,95 +0,2	<b>Fixing tape</b>		
width outside	$B_1$	3,3 max.	width	$W_1$	5,5 ±0,25
pitch	$P$	4,0 ±0,1	thickness	—	0,1 max.
deviation	$\Theta$	15° max.	<b>Carrier tape</b>		
<b>Sprocket hole</b>			width	$W$	8,0 ±0,2
diameter	$D_0$	1,5 +0,1	bending	$\delta$	0,3 max.
pitch	$P_0$	4,0 ±0,1	thickness	$t$	0,4 max.
distance	$E$	1,75 ±0,1	<b>Overall thickness</b>		
cumulative (10)				$K$	1,5 max.
pitch error		±0,1			



7285816

Fig. 2 Configuration of reel and flange (dimensions in mm).

Flange				Hub			
diameter	A	180	tol. +0 -2	diameter	B	62	tol. ± 1,5
thickness	t	1,5	+0,5 -0,1	spindle hole	C	12,75	+0,15 -0
space between flanges	W	9,5	± 0,5	key slit			
				width	E	2	± 0,5
				depth	U	4	± 0,5
				location	O	120	degrees

**Amount of devices per reel**

The bandolier of a 180 mm reel contains at least 2500 devices with no more than 15 empty compartments (0,5%). Three consecutive empty places might be found provided this gap is followed by 6 consecutive devices.

The carrier tape (leader) starts with at least 75 empty positions (equivalent to 300 mm); the covering foil is at least 300 mm. In order to fix the carrier tape a self-adhesive tape of 20 to 50 mm is applied.

At the end of the bandolier (trailer) at least 75 empty positions (equivalent to a length of 300 mm) and 300 mm foil. For fixing onto the reel a self-adhesive tape of 20 to 50 mm is applied.

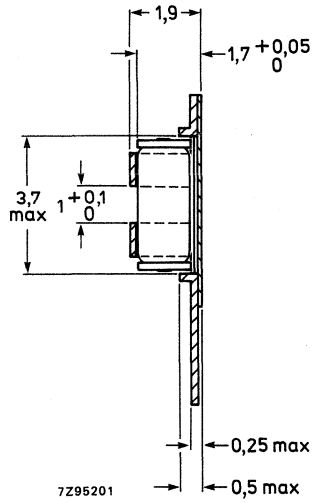


Fig. 3 Cross-sectional view of bandolier with SOD-80 devices.

Note: Testing of SOD-80 devices is possible in this tape. Total number of devices per reel is 2500.



## SOLDERING RECOMMENDATIONS

### SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

#### 1. Flux

A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

#### 2. Metal-alloy solder or solder paste

Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

#### 3. Soldering temperature

This will vary according to the actual method employed.

### REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.

The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C. The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrically arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

### IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:

- a. The temperature of the soldering bath should not exceed 280 °C.
- b. The duration of the soldering cycle should not exceed 10 seconds.
- c. Forced cooling may be applied (see Fig. 1).

### HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.
2. The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.
3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
4. The envelope may be damaged by the iron.

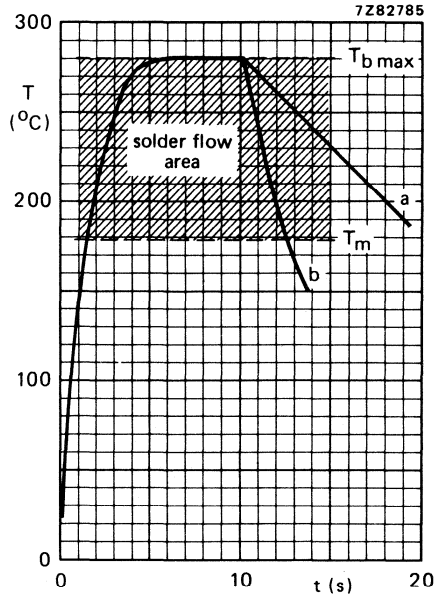


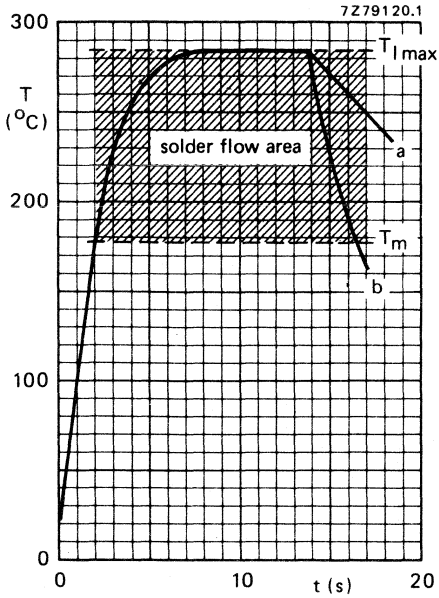
Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.

a = free convection cooling; b = forced cooling.

$T_b \text{ max}$  = maximum bath temperature (280 °C).

$T_m$  = melting temperature of solder (179 °C).



- a = free convection cooling.
- b = permissible forced cooling.
- $T_{l\max}$  = Maximum lead or tab temperature = 285 °C.
- $T_m$  = Melting point of the solder is 179 °C.
- $T_{amb}$  = 25 °C.

Time of heat supply:  
 without preheating max. 14 s  
 with preheating max. 10 s  
 Maximum time of preheating 45 s

Fig. 2 Reflow soldering without preheating.

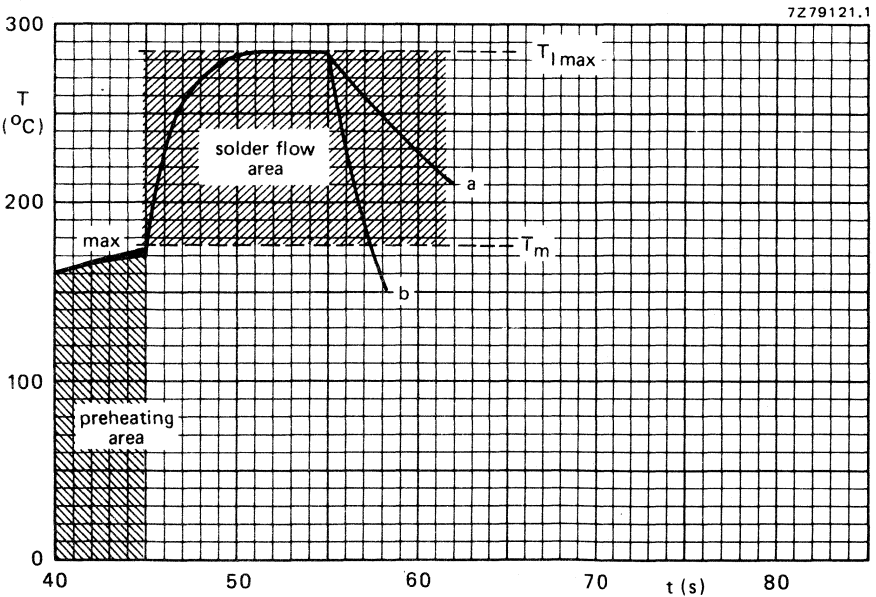


Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal connection pads on hybrid thick and thin-film substrates.

Dimensions in mm

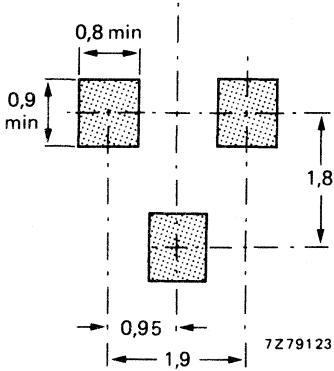


Fig. 4 SOT-23 pattern.

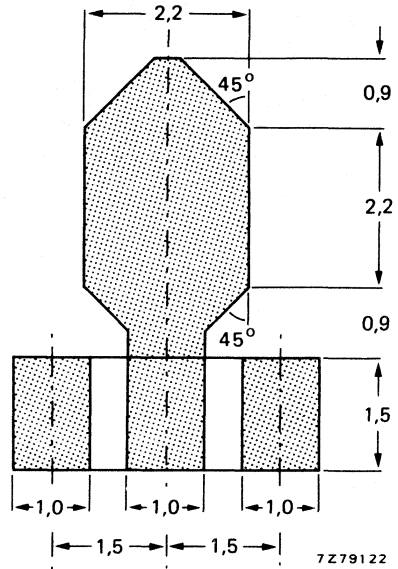


Fig. 5 SOT-89 pattern.

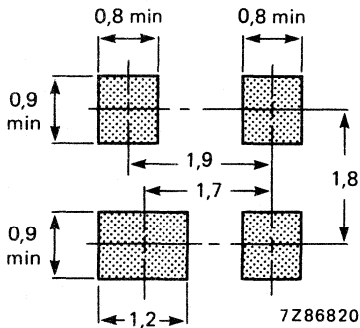


Fig. 6 SOT-143 pattern.



## SOLDERING RECOMMENDATIONS SOT-37 AND SOT-103

Transistors in SOT-37 and SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

### FLAT-LEAD MOUNTING

#### Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the three leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

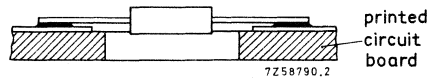


Fig. 1

Solder temperature	max.	300 °C
Soldering time	max.	5 s
Solder-to-case distance	min.	2 mm

### BENT-LEAD MOUNTING

If leads are bent, all three may be soldered simultaneously if desired.

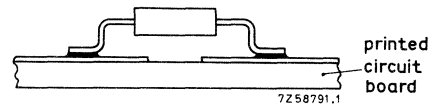


Fig. 2

Solder temperature	max.	300 °C
Soldering time	max.	10 s

### DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

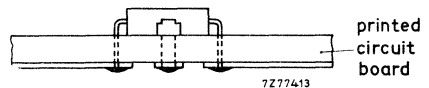


Fig. 3

Solder temperature	max.	260 °C
Soldering time	max.	5 s



## THERMAL CHARACTERISTICS OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).

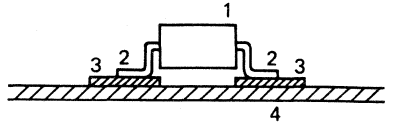
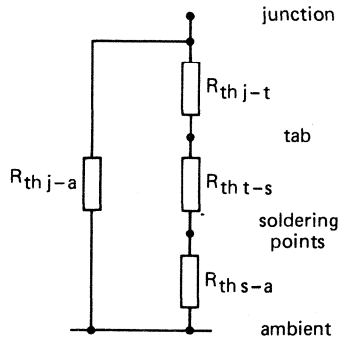


Fig. 1.

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1. Heat radiation from the envelope to ambient (1).  
This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).



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Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed circuit board.

- $R_{th\ j-t}$  = Thermal resistance from junction to tab.  
 $R_{th\ t-s}$  = Thermal resistance from tab to soldering points.  
 $R_{th\ s-a}$  = Thermal resistance from soldering points to ambient.  
 $R_{th\ j-a}$  = Thermal resistance from junction to ambient.

**Heat transfer directly from envelope to ambient**

This depends on the difference between the temperatures of envelope and the surroundings. When the device is mounted on a substrate or printed circuit board direct heat flow can usually be neglected in relation to the heat flow via leads and substrate.

Thus the thermal model can be as in Fig. 3.

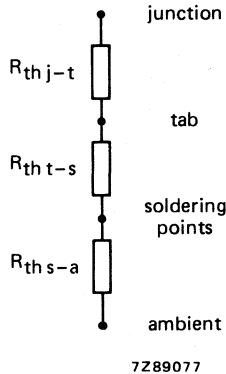


Fig. 3 Basic thermal model.

**Heat transfer from junction to tab**

This is an internal heat transfer and has been measured. In general it is:

- for high-frequency transistors, low-power diodes and (MOS) FETs 60 K/W
- for low-frequency and switching transistors 50 K/W
- for low-frequency medium-power transistors 30 K/W

**Heat transfer from tab to soldering points**

- This value has also been measured for SOT-23 with  $P_{tot} < 350\text{ mW}$  280 K/W
- for types of semiconductors in this envelope with  $P_{tot} < 425\text{ mW}$  260 K/W
- for types of semiconductors in a SOT-143 envelope this value is 310 K/W

**Heat transfer from soldering points to ambient**

This depends on the shape and material of tracks and substrate. In figures 4 and 5 standard mounting conditions are given to set up the maximum power ratings for SOT-23 and SOT-143 encapsulations.

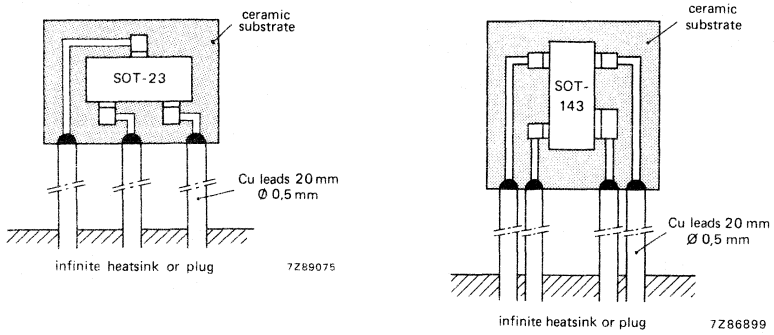


Fig. 4 Test circuits SOT-23 and SOT-143 mounting conditions on a ceramic substrate.

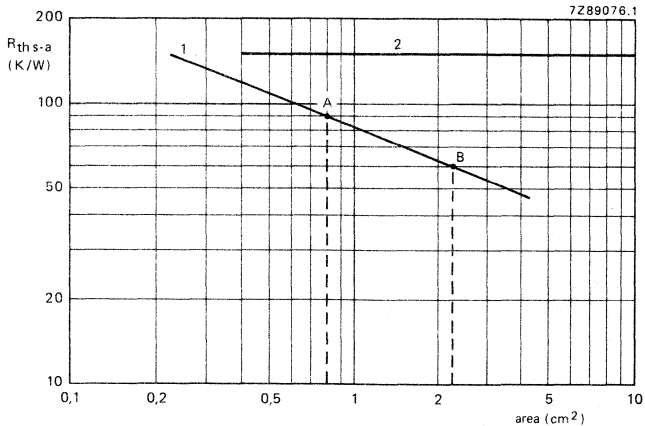


Fig. 5 Heat transfer from soldering points to ambient.

**1. Ceramic substrate**

Point A on the curve in Fig. 5 is for an area of the ceramic substrate of 8 mm x 10 mm x 0,7 mm for the maximum rating of all high-frequency, low-frequency and switching transistors and also for all diodes.

Point B on the curve in Fig. 5 is for an area of the ceramic substrate of 15 mm x 15 mm x 0,7 mm for the maximum rating of low-frequency medium-power semiconductors.

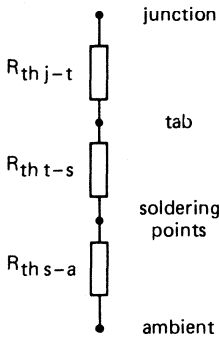
**2. Printed circuit board**

$R_{th\ s-a} = 150\ K/W$  for SOT-23 and SOT-143 envelopes mounted on a printed circuit board.

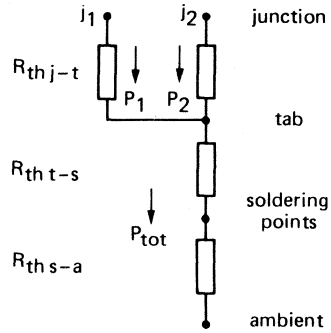
The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned in Figs 3 and 5.

The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$$



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Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot (R_{th\ t-s} + R_{th\ s-a}) + T_{amb} = P_{tot} (280 + 90) + T_{amb}$$

$$T_{j1} = (P_1 \times R_{th\ j-t}) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = (P_2 \times R_{th\ j-t}) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j-t}$  for diodes is 60 K/W.

$R_{th\ s-a}$  (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t-s}$  for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60 P_1 + 370 P_{tot} + T_{amb}$$

$$T_{j2} = 60 P_2 + 370 P_{tot} + T_{amb}$$

**DEVICE DATA**

**J-FETS**





## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

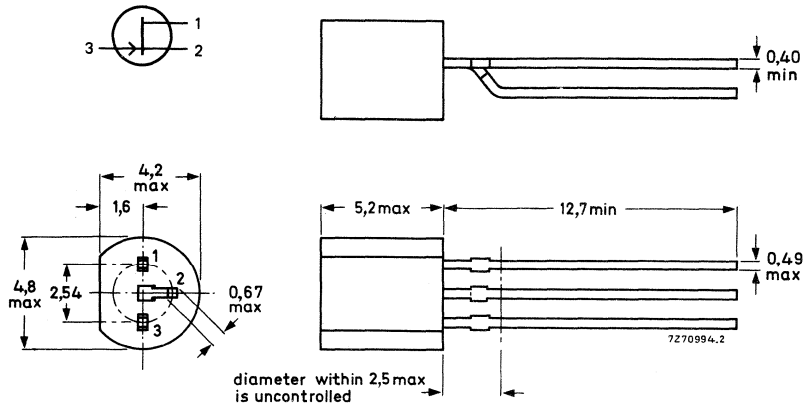
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$		2 to 12 mA
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ Y_{fs} $	typ.	3,5 mA/V
Noise figure at $V_{DS} = 15\text{ V}; V_{GS} = 0$ $f = 1\text{ kHz}; R_G = 1\text{ M}\Omega$	F	<	2 dB

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V

Current

Gate current	$I_G$	max.	10	mA
--------------	-------	------	----	----

Power dissipation

Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300	mW
--	-----------	------	-----	----

Temperatures

Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}\text{C}$
Junction temperature	$T_j$	max. 150	$^{\circ}\text{C}$

**THERMAL RESISTANCE**

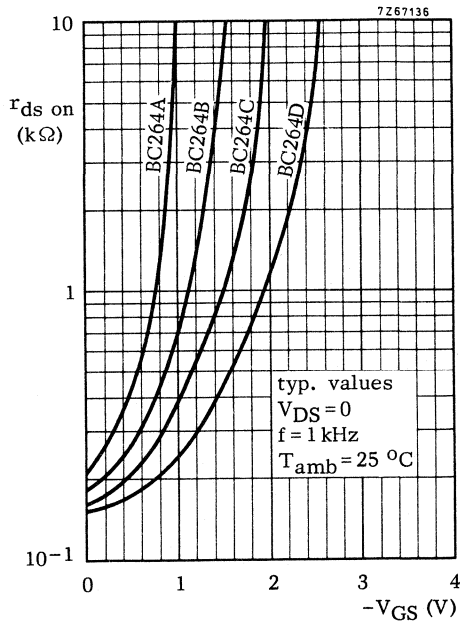
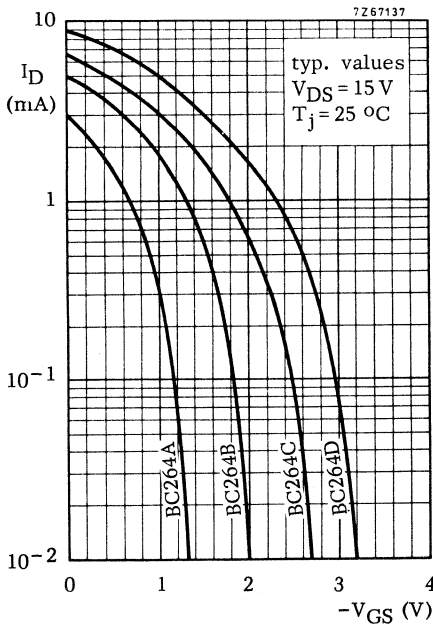
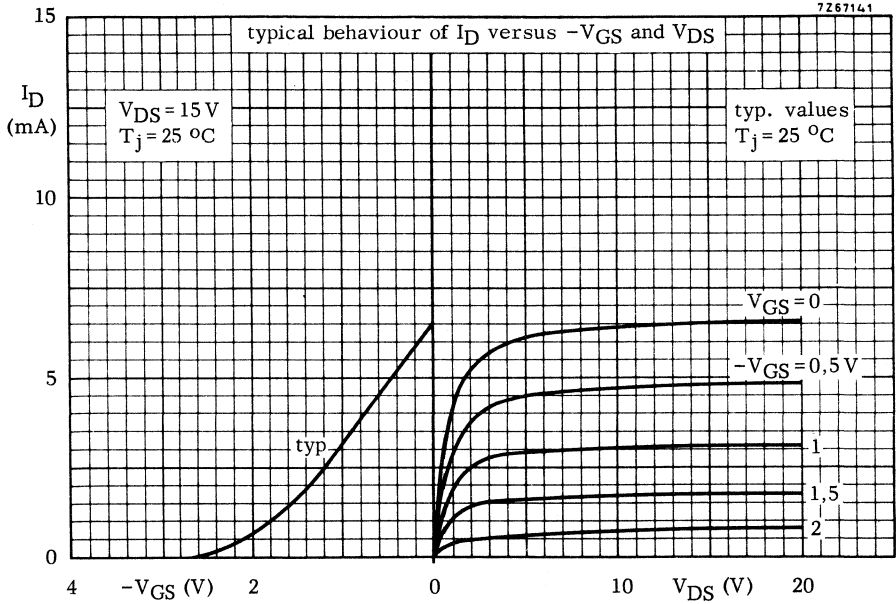
From junction to ambient in free air	$R_{th\ j-a}$	=	0,42	$^{\circ}\text{C}/\text{mW}$
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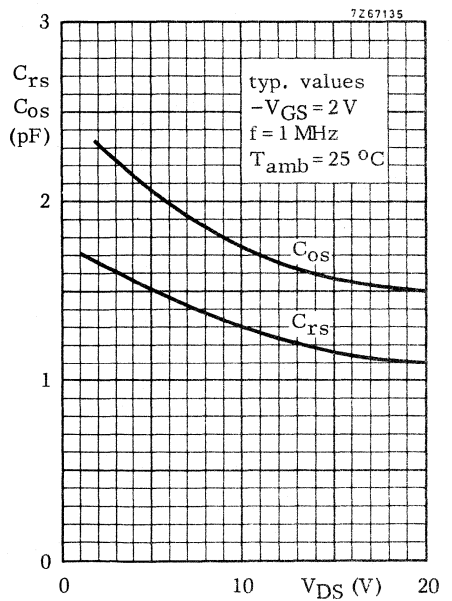
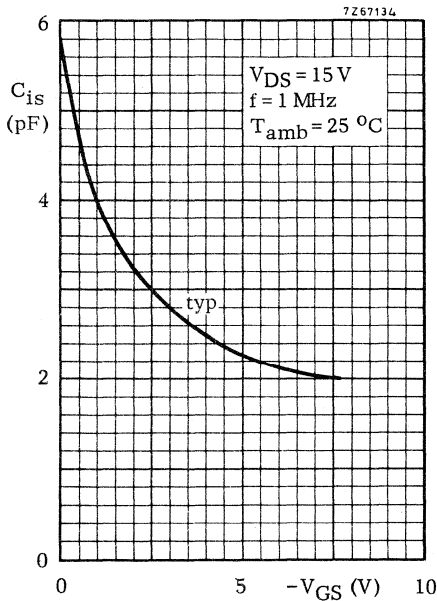
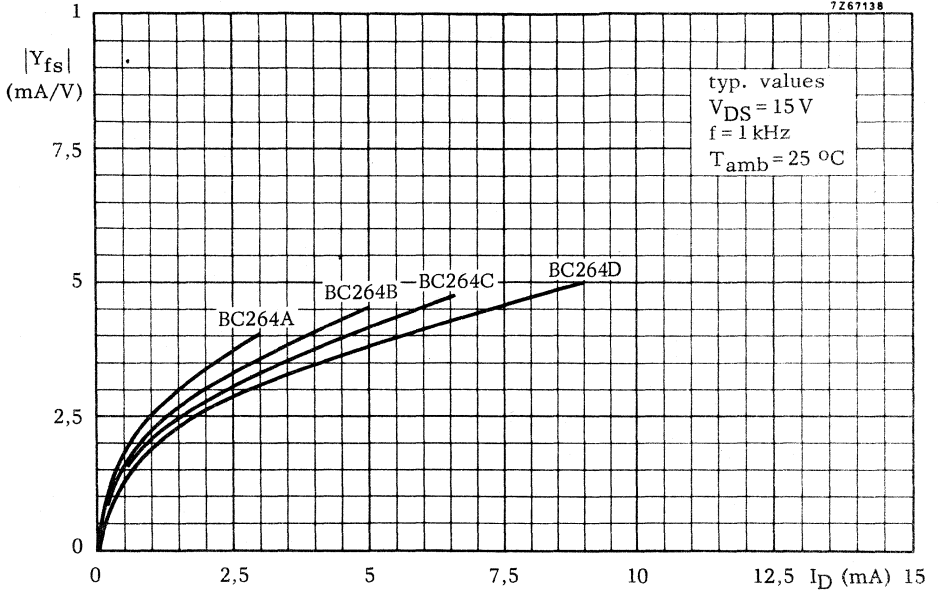
**CHARACTERISTICS**

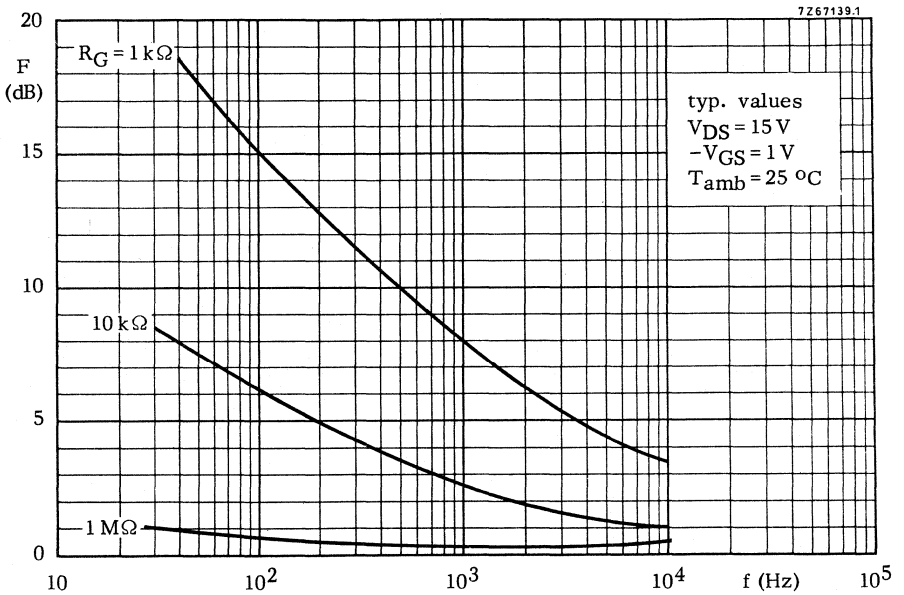
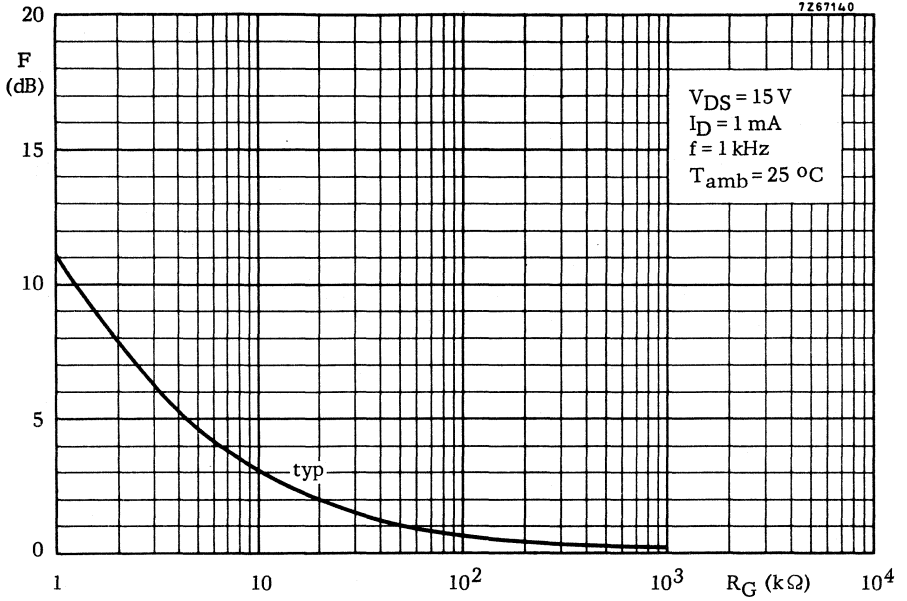
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

		BC264A	B	C	D	
<u>Gate cut-off current</u>						
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	< 10	10	10	10	nA
<u>Drain current</u> 1)						
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	> 2,0 < 4,5	3,5 6,5	5,0 8,0	7,0 12,0	mA mA
<u>Gate-source breakdown voltage</u>						
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	> 30	30	30	30	V
<u>Gate-source voltage</u>						
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> 0,4	0,4	0,4	0,4	V
$I_D = 1,0\text{ mA}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> 0,2 < 1,2	- -	- -	- -	V V
$I_D = 1,5\text{ mA}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> - < -	0,4 1,4	- -	- -	V V
$I_D = 2,5\text{ mA}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> - < -	- -	0,5 1,5	- -	V V
$I_D = 3,5\text{ mA}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> - < -	- -	- -	0,6 1,6	V V
<u>Gate-source cut-off voltage</u>						
$I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	> 0,5	0,5	0,5	0,5	V
<u>y-parameters</u> at $T_{amb} = 25\text{ }^\circ\text{C}$						
$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	Transfer admittance	$ y_{fs} $	> 2,5	3,0	3,5	4,0 mA/V
$V_{DS} = 15\text{ V}; -V_{GS} = 1\text{ V}; f = 1\text{ MHz}$	Input capacitance	$C_{is}$	typ.	4,0		pF
	Feedback capacitance	$C_{rs}$	typ.	1,2		pF
	Output capacitance	$C_{os}$	typ.	1,6		pF
<u>Noise figure</u> at $f = 1\text{ kHz}; R_G = 1\text{ M}\Omega$						
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}$	F		typ. <	0,5 2		dB dB
<u>Equivalent noise voltage</u> at $T_{amb} = 25\text{ }^\circ\text{C}$						
$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 10\text{ Hz}$	$V_n/\sqrt{B}$	typ.		40		nV/ $\sqrt{\text{Hz}}$

1) Measured under pulse conditions.







## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

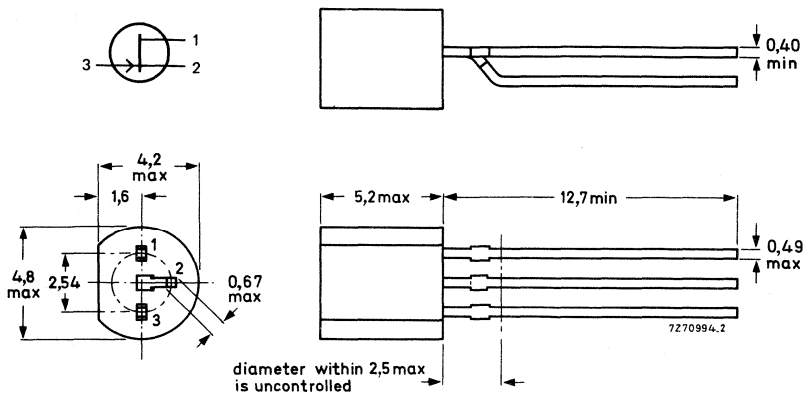
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V		
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V		
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW		
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	BF245A/0				
		A	B	C	
$I_{DSS}$	>	0,5	1,9	6	12 mA
	<	2,1	6,5	15	25 mA
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	0,25 to 8,0 V			
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 20\text{ V}; -V_{GS} = 1\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	$C_{rs}$	typ.	1,1 pF		
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$	$ Y_{fs} $	3,0 to 6,5 mS			

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	$I_D$	max.	25 mA
Gate current	$I_G$	max.	10 mA
Power dissipation			
up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
up to $T_{amb} = 90\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW 1)
Storage temperature	$T_{stg}$		$-65$ to $+150\text{ }^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

## THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,25 K/mW
From junction to ambient	$R_{th\ j-a}$	=	0,20 K/mW 1)

## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off current		BF245A	B	C
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	< 5	5	5 nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 125\text{ }^\circ\text{C}$	$-I_{GSS}$	< 0,5	0,5	0,5 $\mu\text{A}$
Drain current 2)				
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS\ 3)}$	> 2	6,0	12 mA
		< 6,5	15,0	25 mA
Gate-source breakdown voltage				
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	> 30	30	30 V
Gate-source voltage				
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS\ 3)}$	> 0,4	1,6	3,2 V
		< 2,2	3,8	7,5 V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions:  $t_p = 300\text{ }\mu\text{s}; \delta \leq 0,02$ .

- 3) BF245A/0:  $I_{DSS} = 0,5$  to  $2,1\text{ mA}; -V_{GS} = 0,2$  to  $1,0\text{ V}$   
 → BF245A/1:  $I_{DSS} = 1,9$  to  $3,0\text{ mA}; -V_{GS} = 0,4$  to  $1,0\text{ V}$   
 BF245A/2:  $I_{DSS} = 3,0$  to  $4,5\text{ mA}; -V_{GS} = 0,7$  to  $1,4\text{ V}$   
 BF245A/3:  $I_{DSS} = 4,5$  to  $6,5\text{ mA}; -V_{GS} = 1,1$  to  $2,2\text{ V}$ .



## Gate-source cut-off voltage

$I_D = 10 \text{ nA}; V_{DS} = 15 \text{ V}$

$-V_{(P)GS} \quad 0,25 \text{ to } 8,0 \text{ V}$

y-parameters at  $T_{amb} = 25 \text{ }^\circ\text{C}$  (common source)

$V_{DS} = 15 \text{ V}; V_{GS} = 0$

$f = 1 \text{ kHz}$

Transfer admittance

$|Y_{fs}| \quad 3,0 \text{ to } 6,5 \text{ mS}$

Output admittance

$|Y_{os}| \quad \text{typ. } 25 \text{ } \mu\text{S}$

$f = 200 \text{ MHz}$

Input conductance

$g_{is} \quad \text{typ. } 250 \text{ } \mu\text{S}$

Reverse transfer admittance

$|Y_{rs}| \quad \text{typ. } 1,4 \text{ mS}$

Transfer admittance

$|Y_{fs}| \quad \text{typ. } 6 \text{ mS}$

Output conductance

$g_{os} \quad \text{typ. } 40 \text{ } \mu\text{S}$

$V_{DS} = 20 \text{ V}; -V_{GS} = 1 \text{ V}$

$f = 1 \text{ MHz}$

Input capacitance

$C_{is} \quad \text{typ. } 4,0 \text{ pF}$

Feedback capacitance

$C_{rs} \quad \text{typ. } 1,1 \text{ pF}$

Output capacitance

$C_{os} \quad \text{typ. } 1,6 \text{ pF}$

## Cut-off frequency \*

$V_{DS} = 15 \text{ V}; V_{GS} = 0$

$f_{gfs} \quad \text{typ. } 700 \text{ MHz}$

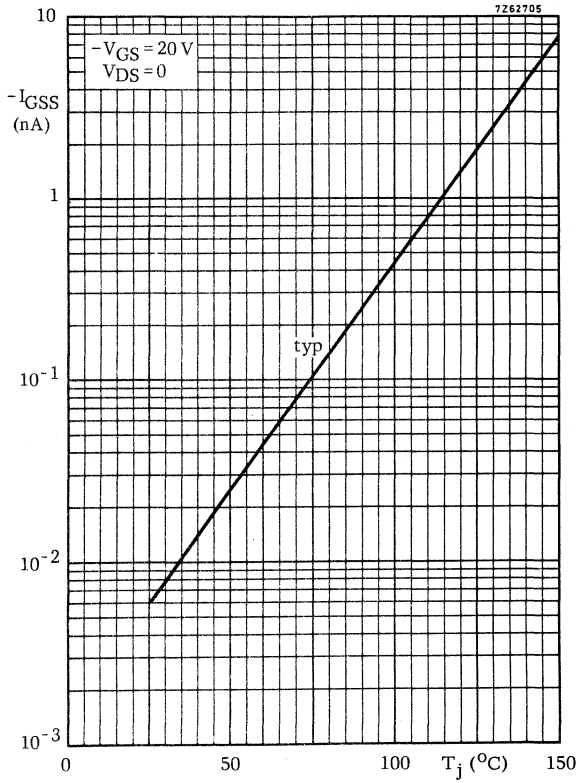
Noise figure at  $f = 100 \text{ MHz}; R_G = 1 \text{ k}\Omega$  (common source)

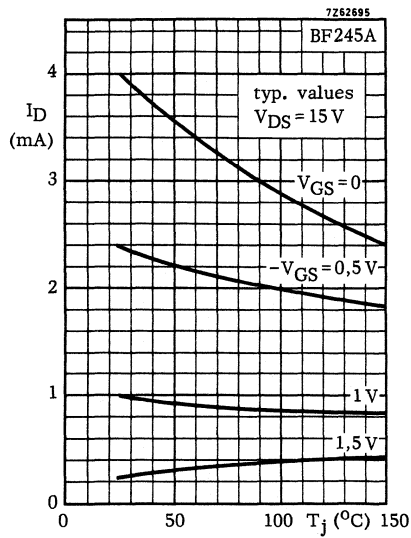
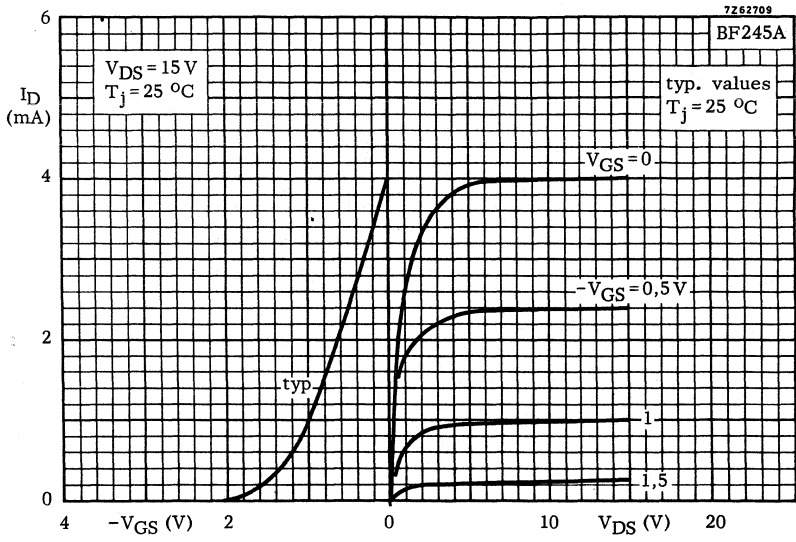
$V_{DS} = 15 \text{ V}; V_{GS} = 0; T_{amb} = 25 \text{ }^\circ\text{C}$

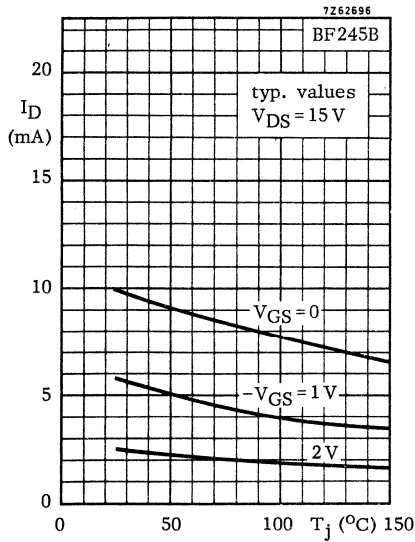
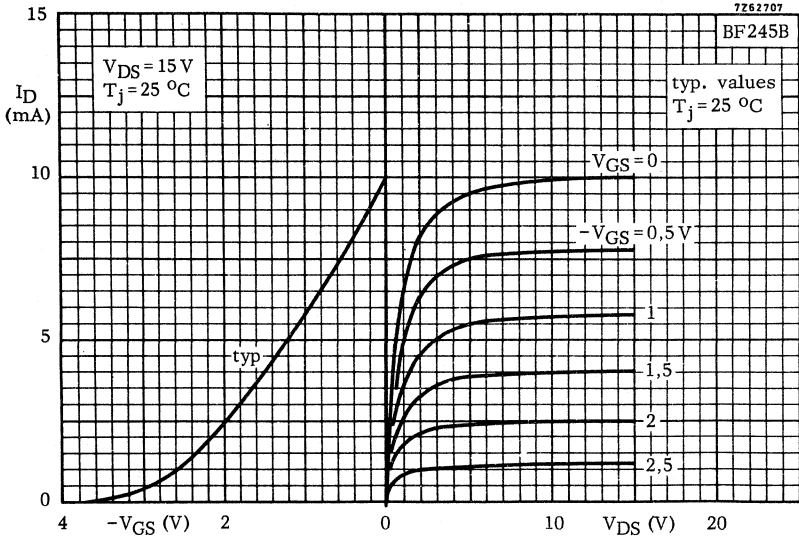
input tuned to minimum noise

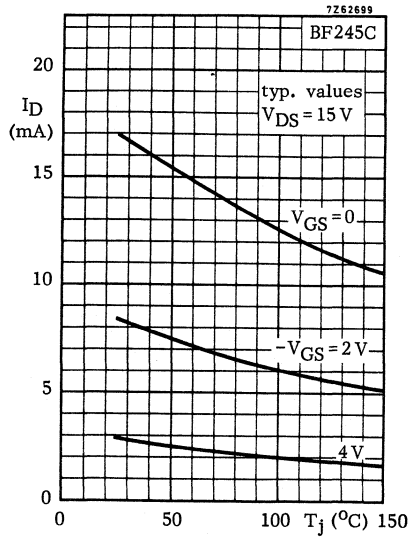
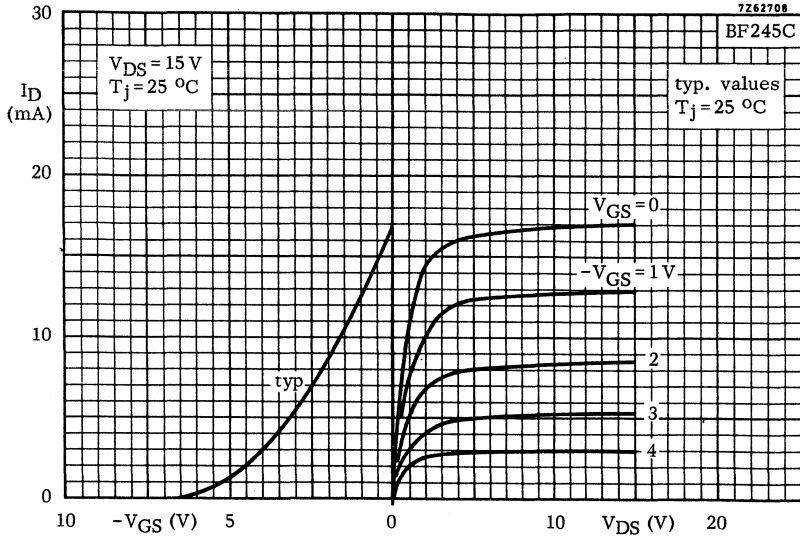
$F \quad \text{typ. } 1,5 \text{ dB}$

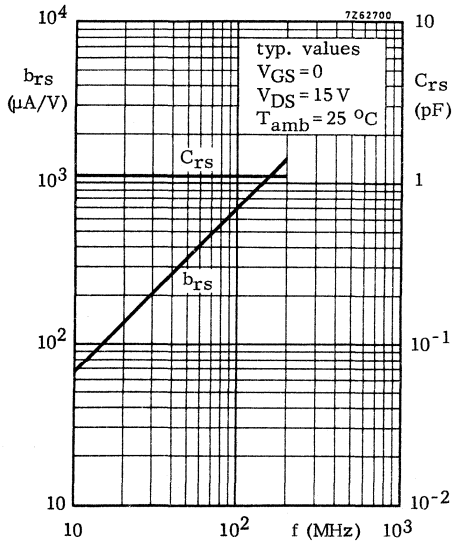
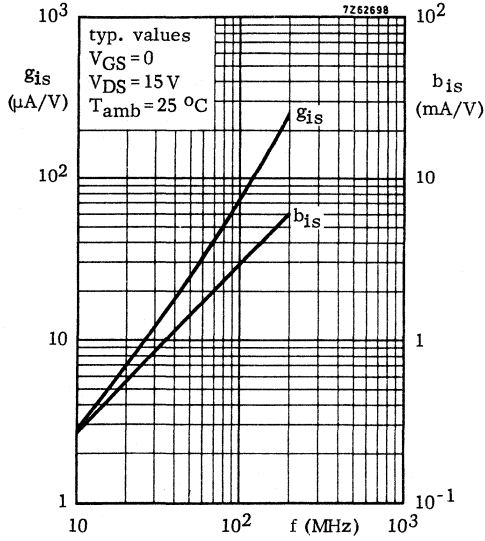
\* The frequency at which  $g_{fs}$  is 0,7 of its value at 1 kHz.

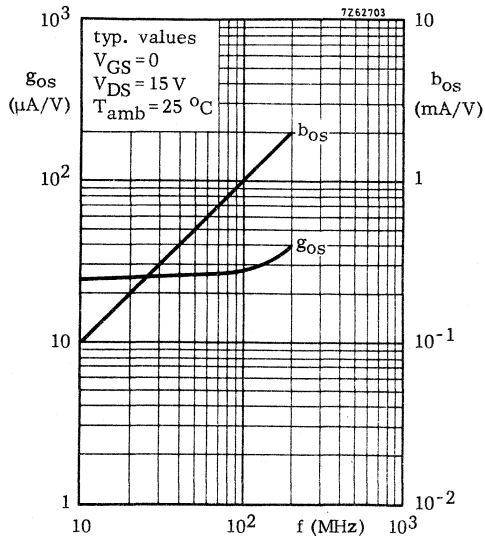
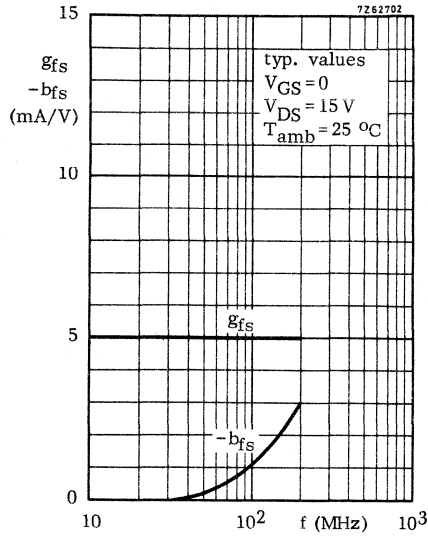


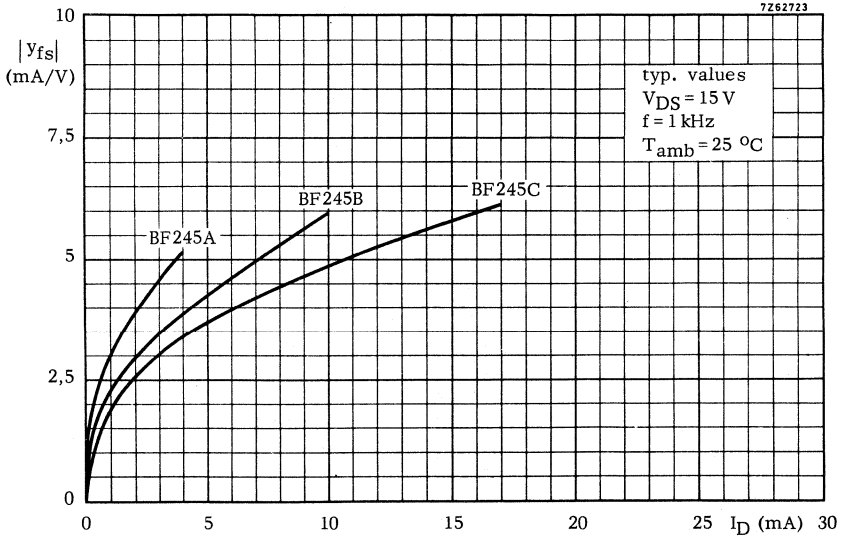
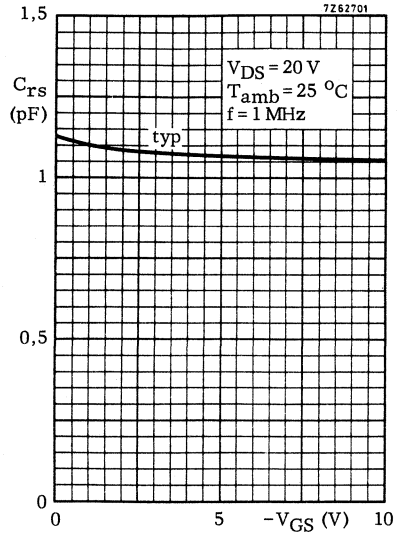
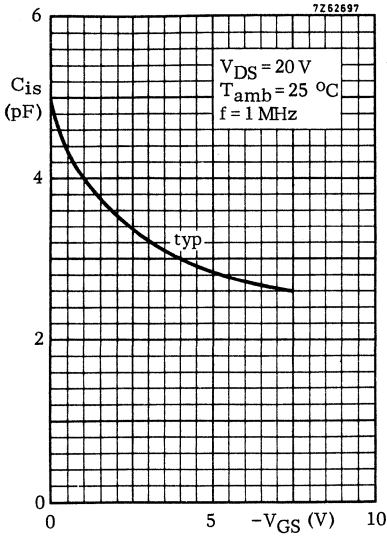




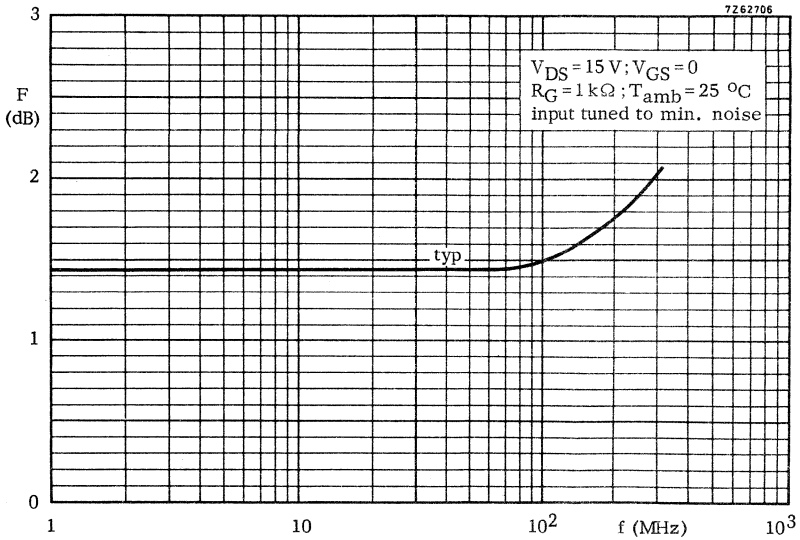
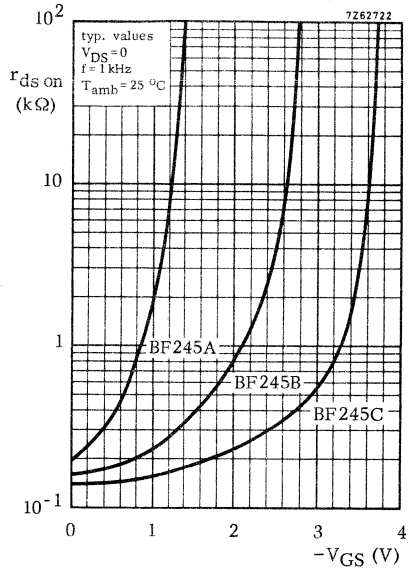
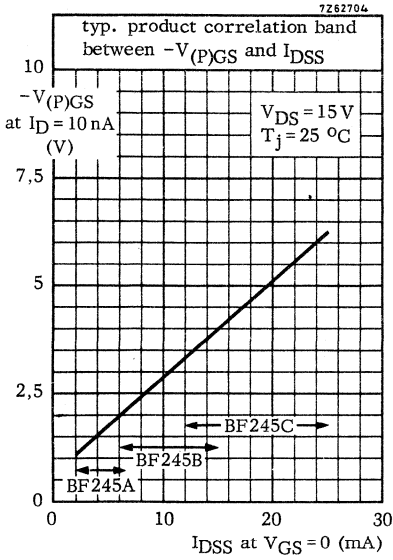














## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for v.h.f. and u.h.f. amplifiers, mixers, and general purpose switching.

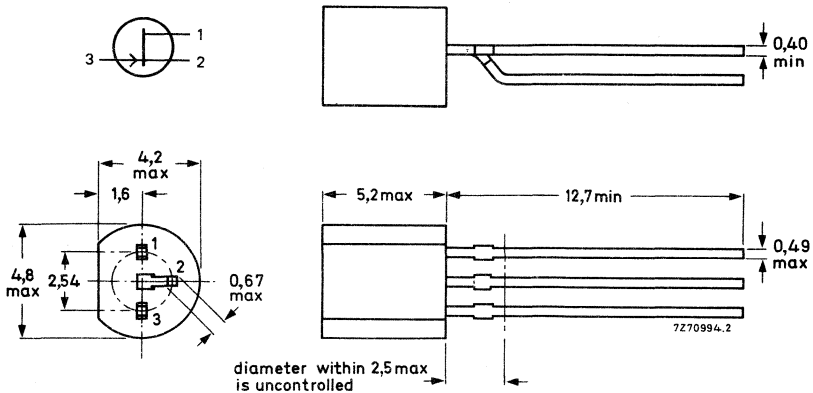
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V	
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	250 mW	
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	BF247A	B	C
		> 30	60	110 mA
		< 80	140	250 mA
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V(P)GS$		0,6 to 14,5 V	
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}$	$C_{rs}$	typ.	3,5 pF	
Transfer admittance (common source) $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	>	8 mS	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate current	$I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	250 mW
Storage temperature	$T_{stg}$		-65 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W
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**CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$

		BF247A	B	C	
Gate cut-off current $-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS}$	< 5	5	5 nA	
Drain current* $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	> 30	60	110 mA	
		< 80	140	250 mA	
Gate-source breakdown voltage $-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	> 25	25	25 V	
Gate-source voltage $I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> 1,5	3,0	5,5 V	
		< 4,0	7,0	12,0 V	
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$		0,6 to 14,5 V		
Transfer admittance (common source) $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	>		8 mS	
		typ.		17 mS	
Capacitances at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}$	$C_{rs}$	typ.		3,5 pF	
		input capacitance	$C_{is}$	typ.	11 pF
		output capacitance	$C_{cs}$	typ.	5 pF
Cut-off frequency** $V_{DS} = 15\text{ V}; V_{GS} = 0$	$f_{gfs}$	typ.		450 MHz	

\* Measured under pulse conditions;  $t_p = 300\text{ }\mu\text{s}; \delta \leq 0,02$ .

\*\* The frequency at which  $g_{fs}$  is 0,7 of its value at 1 kHz.

## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

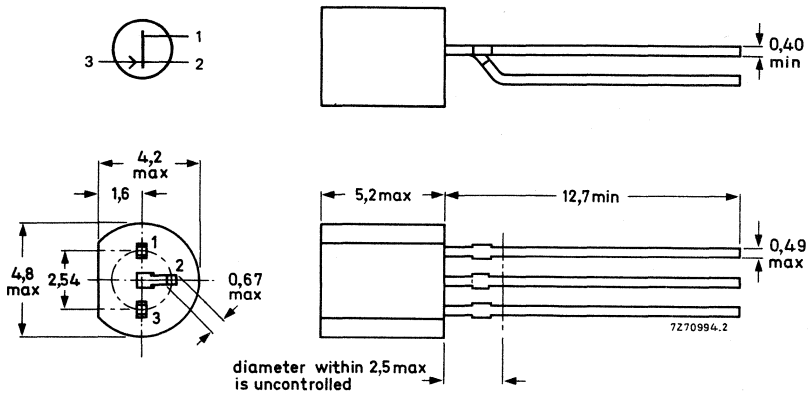
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V	
Gate-source voltage (open drain)	$-V_{GS0}$	max.	30 V	
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW	
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	BF256A	B	C
		$> 3$	6	11 mA
		$< 7$	13	18 mA
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 20\text{ V}; -V_{GS} = 1\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	$C_{rs}$	typ.	0,7 pF	
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$	$ Y_{fs} $	$>$	4,5 mS	
Power gain at $f = 800\text{ MHz}$ $V_{DS} = 15\text{ V}; R_S = 47\text{ }\Omega$	$G_p$	typ.	11 dB	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	$I_G$	max.	10 mA
Total power dissipation			
up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
up to $T_{amb} = 90\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW 1)
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{thj-a}$	=	0,25 K/mW
From junction to ambient	$R_{thj-a}$	=	0,20 K/mW 1)

**CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off current				
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	5 nA	
Drain current 2)				
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS\ 3)}$		BF256A	B   C
		>	3	6   11 mA
		<	7	13   18 mA
Gate-source breakdown voltage				
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	>	30 V	
Gate-source voltage				
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS\ 3)}$		0,5 to 7,5 V	

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions:  $t_p = 300\text{ }\mu\text{s}; \delta \leq 0,02$ .

3) BF256B/1:  $I_{DSS} = 6\text{ to }8\text{ mA}; -V_{GS} = 1,4\text{ to }2,6\text{ V}$ .

## y-parameters (common source)

Transistor admittance at  $f = 1$  kHz

$$V_{DS} = 15 \text{ V}; V_{GS} = 0$$

$ y_{fs} $	>	4,5 mS 1)
	typ.	5 mS 1)

Output capacitance at  $f = 1$  MHz

$$V_{DS} = 20 \text{ V}; V_{GS} = 0$$

$C_{OS}$	typ.	1,2 pF
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Feedback capacitance at  $f = 1$  MHz

$$V_{DS} = 20 \text{ V}; -V_{GS} = 1 \text{ V}$$

$C_{RS}$	typ.	0,7 pF
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Cut-off frequency

$$V_{DS} = 15 \text{ V}; V_{GS} = 0$$

$f_{gfs}$	typ.	1 GHz 2)
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Noise figure at  $f = 800$  MHz

$$V_{DS} = 10 \text{ V}; R_S = 47 \Omega$$

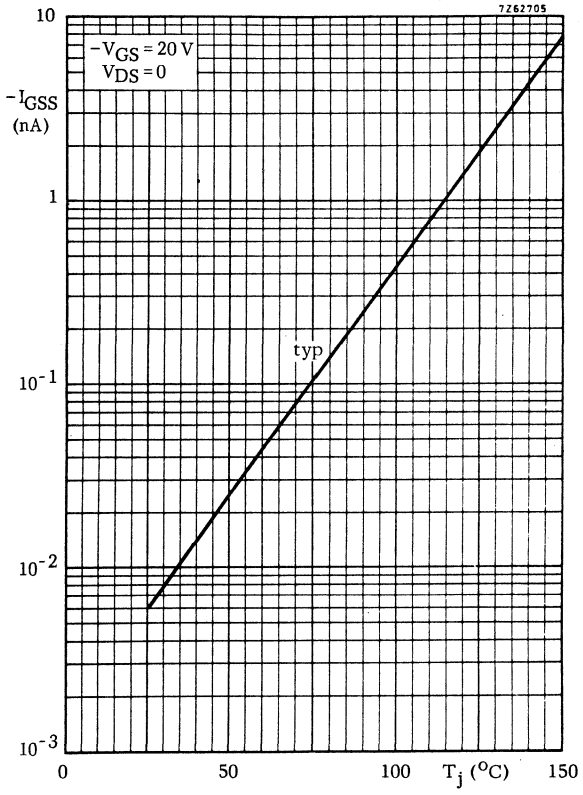
F	typ.	7,5 dB
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Power gain at  $f = 800$  MHz

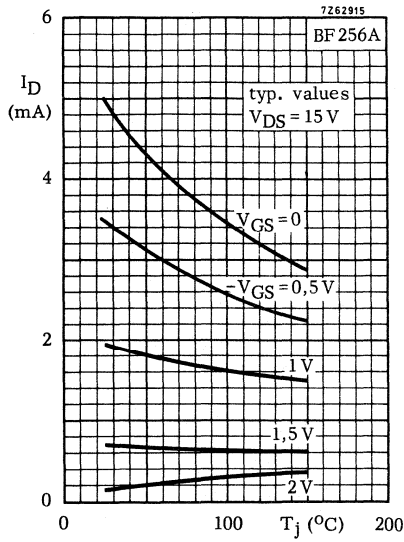
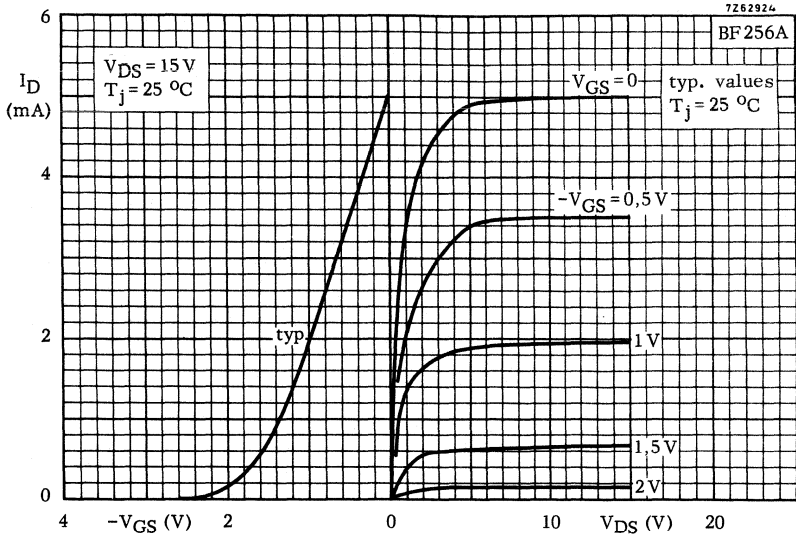
$$V_{DS} = 15 \text{ V}; R_S = 47 \Omega$$

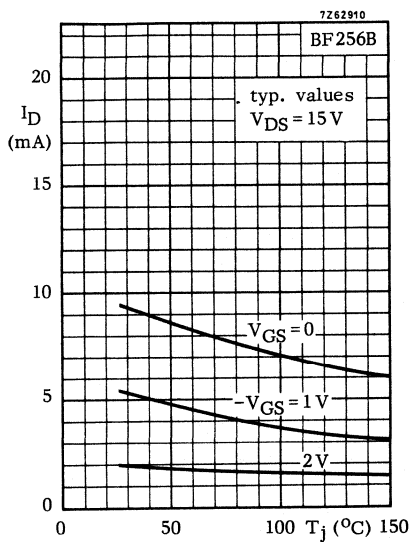
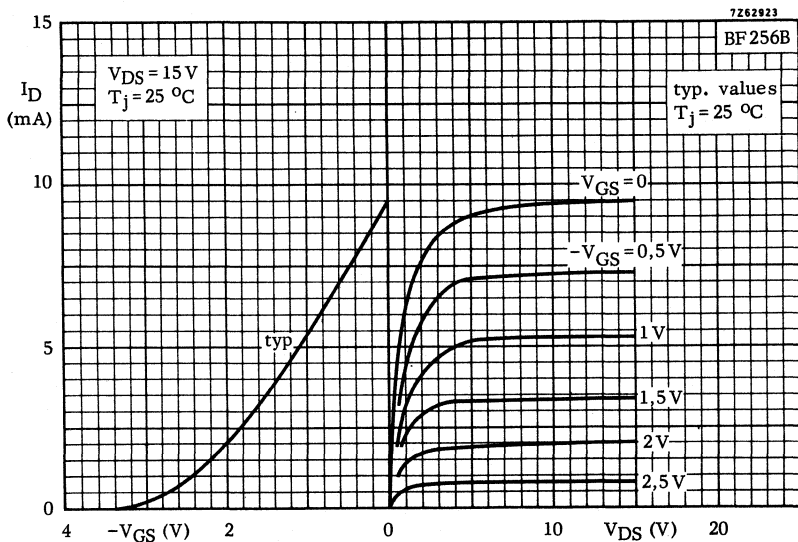
$G_p$	typ.	11 dB
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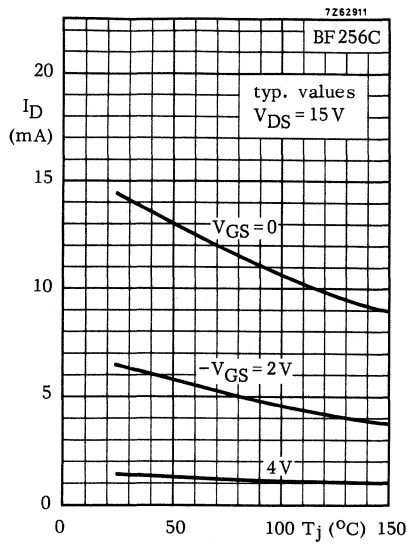
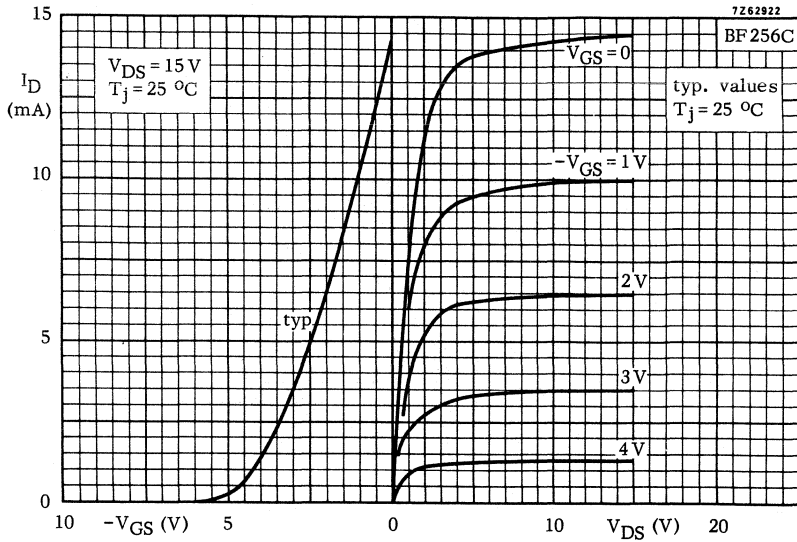
1) Measured under pulse conditions:  $t_p = 300 \mu s$ ;  $\delta \leq 0,02$ .2) The frequency at which  $g_{fs}$  is 0,7 of its value at 1 kHz.

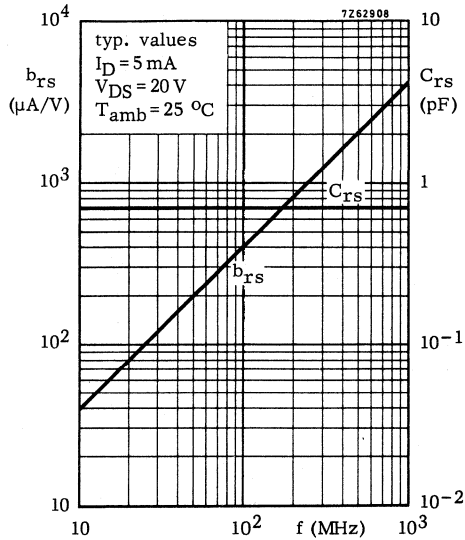
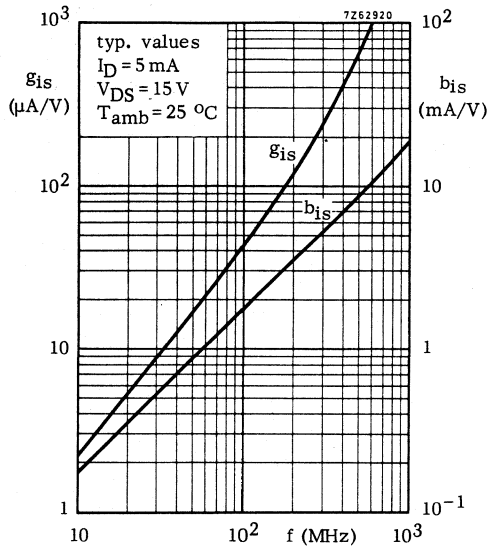


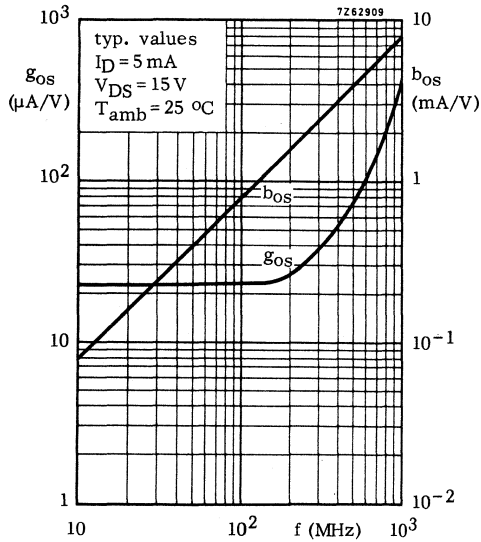
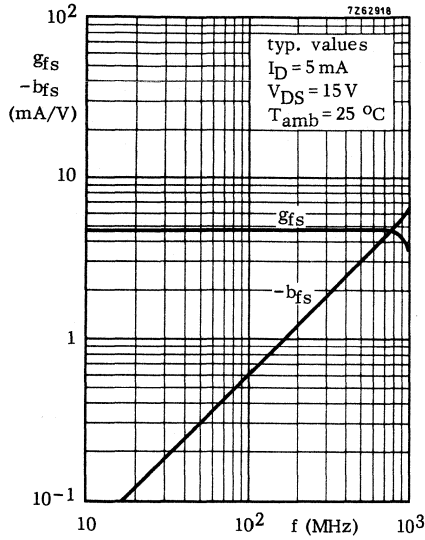


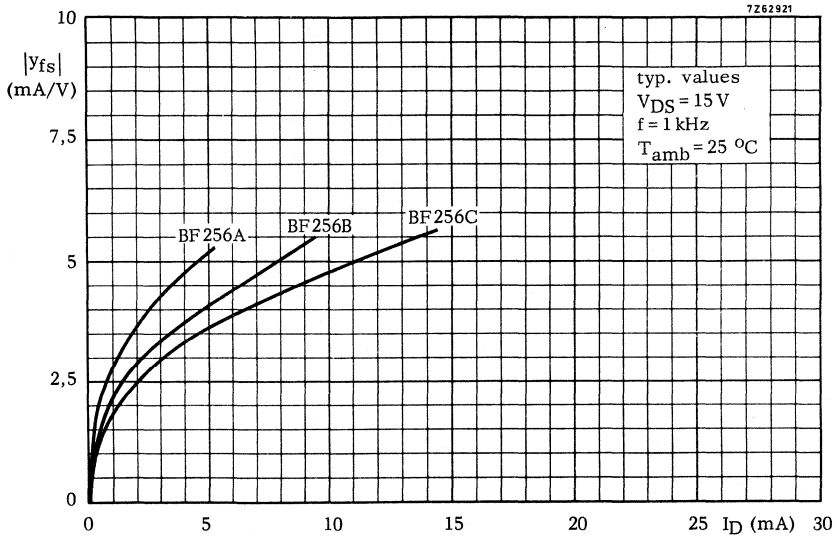
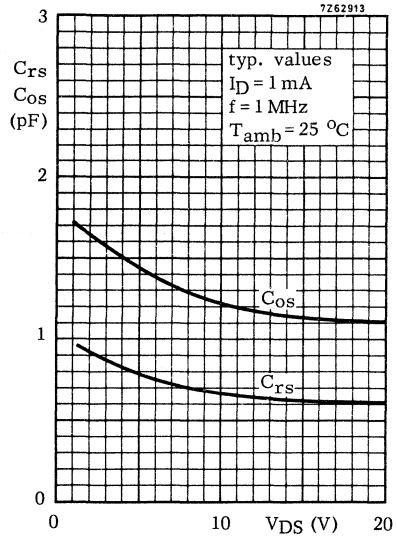
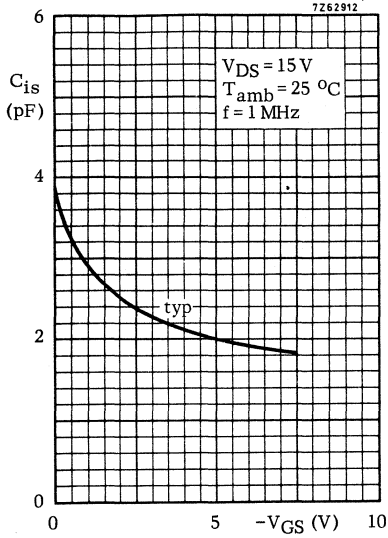


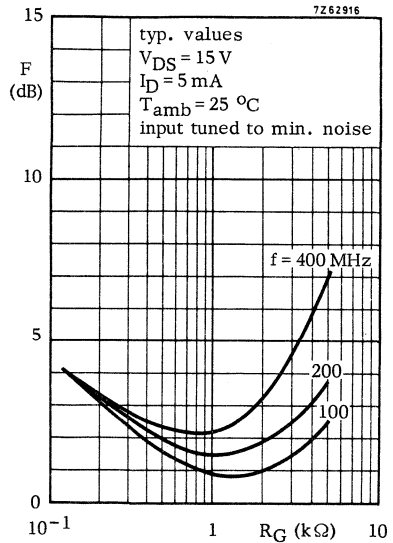
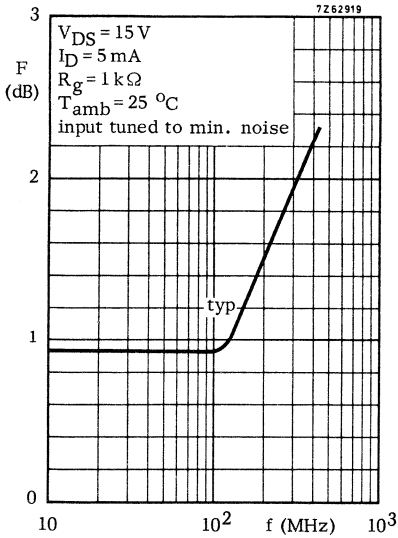
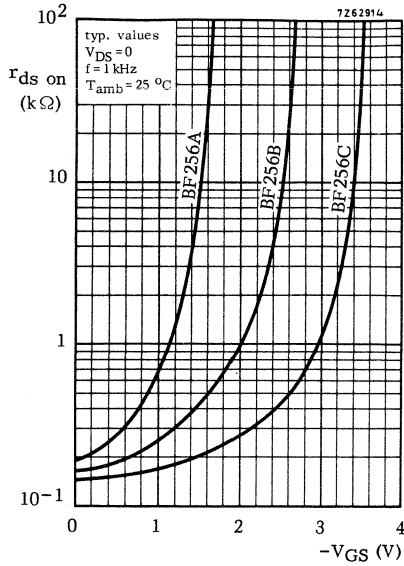
















## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the v.h.f. range.

These FETs can be supplied in four  $I_{DSS}$  groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the r.f. stages in f.m. portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

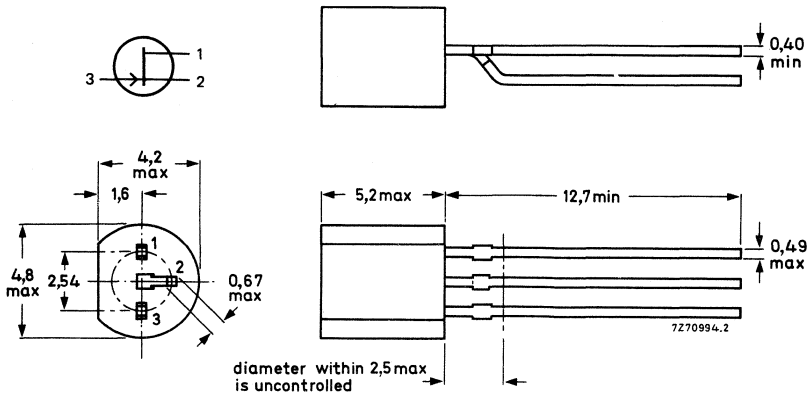
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20	V			
Drain current (d.c. or average)	$I_D$	max.	30	mA			
Total power dissipation up to $T_{amb} = 75^\circ\text{C}$	$P_{tot}$	max.	300	mW			
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$		BF410A	B	C	D	
		$>$	0,7	2,5	6	10	mA
		$<$	3,0	7,0	12	18	mA
Transfer admittance (common source) $V_{DS} = 10\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ y_{fs} $	$>$	2,5	4	6	7	mS
Feedback capacitance $V_{DS} = 10\text{ V}; V_{GS} = 0$ $V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	$C_{rs}$	typ.	0,3	0,3	—	—	pF
	$C_{rs}$	typ.	—	—	0,3	0,3	pF
Noise figure at optimum source admittance $G_S = 1\text{ mS}; -B_S = 3\text{ mS}; f = 100\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$ $V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	F	typ.	1,5	1,5	—	—	dB
	F	typ.	—	—	1,5	1,5	dB

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	30 mA
Gate current	$\pm I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

→ From junction to ambient in free air

$$R_{th\ j-a} = 0,25\ \text{K/mW}$$

**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$

Gate cut-off current

$$-V_{GS} = 0,2\ \text{V}; V_{DS} = 0$$

$-I_{GSS}$	<	BF410A	B	C	D	
		10	10	10	10	nA

Gate-drain breakdown voltage

$$I_S = 0; -I_D = 10\ \mu\text{A}$$

$-V_{(BR)GDO}$	>	20	20	20	20	V
----------------	---	----	----	----	----	---

Drain current

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$I_{DSS}$	>	0,7	2,5	6	10	mA
	<	3,0	7,0	12	18	mA

Gate-source cut-off voltage

$$I_D = 10\ \mu\text{A}; V_{DS} = 10\ \text{V}$$

$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V
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## DYNAMIC CHARACTERISTICS

Measuring conditions (common source):  $V_{DS} = 10 \text{ V}$ ;  $V_{GS} = 0$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$  for BF410A and B  
 $V_{DS} = 10 \text{ V}$ ;  $I_D = 5 \text{ mA}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$  for BF410C and D

## y-parameters (common source)

		BF410A	B	C	D	
Input capacitance at $f = 1 \text{ MHz}$	$C_{is} <$	5	5	5	5 pF	
Input conductance at $f = 100 \text{ MHz}$	$g_{is} \text{ typ.}$	100	90	60	50 $\mu\text{S}$	
Feedback capacitance at $f = 1 \text{ MHz}$	$C_{rs} \text{ typ.}$	0,3	0,3	0,3	0,3 pF	
	$C_{rs} <$	0,4	0,4	0,4	0,4 pF	
Transfer admittance at $f = 1 \text{ kHz}$ $V_{GS} = 0$ instead of $I_D = 5 \text{ mA}$	$ y_{fs}  >$	2,5	4,0	4,0	3,5 mS	
	$ y_{fs}  >$	—	—	6,0	7,0 mS	
Transfer admittance at $f = 100 \text{ MHz}$	$ y_{fs}  \text{ typ.}$	3,5	5,5	5,0	5,0 mS	
Output capacitance at $f = 1 \text{ MHz}$	$C_{os} <$	3	3	3	3 pF	
Output conductance at $f = 1 \text{ MHz}$	$g_{os} <$	60	80	100	120 $\mu\text{S}$	
Output conductance at $f = 100 \text{ MHz}$	$g_{os} \text{ typ.}$	35	55	70	90 $\mu\text{S}$	
Noise figure at optimum source admittance $G_S = 1 \text{ mS}$ ; $-B_S = 3 \text{ mS}$ ; $f = 100 \text{ MHz}$	F	typ.	1,5	1,5	1,5	1,5 dB

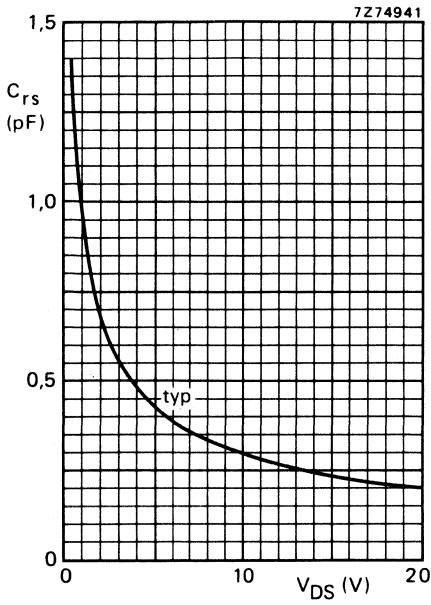


Fig. 2  $V_{GS} = 0$  for BF410A and BF410B;  
 $I_D = 5$  mA for BF410C and BF410D;  
 $f = 1$  MHz;  $T_{amb} = 25$  °C.

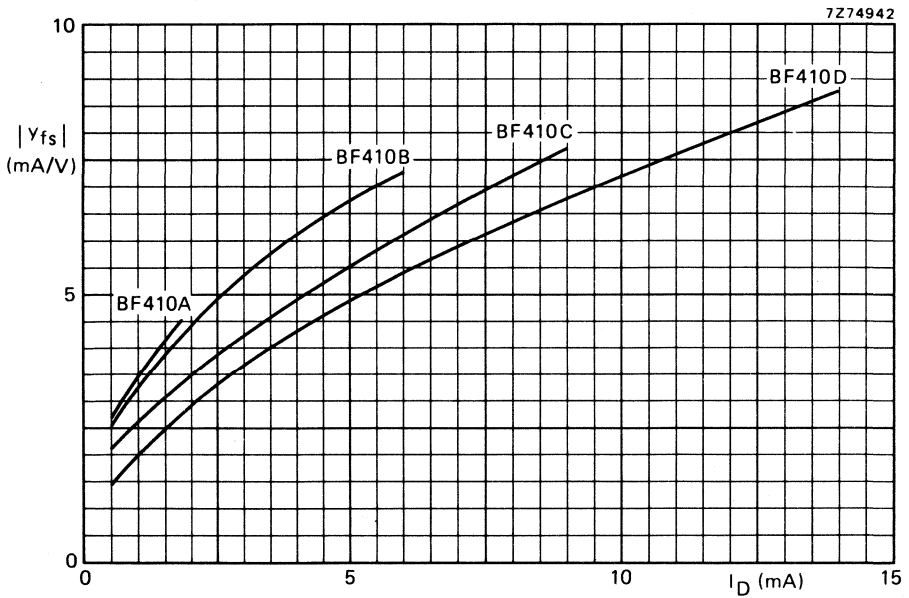


Fig. 3  $V_{DS} = 10$  V;  $f = 1$  kHz;  $T_{amb} = 25$  °C; typical values.

## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20			V
Drain current (d.c. or average)	$I_D$	max.	30			mA
Total power dissipation up to $T_{amb} = 65\text{ }^\circ\text{C}$	$P_{tot}$	max.	250			mW
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	0,7	2,5	6	10 mA
		<	3,0	7,0	12	18 mA
Transfer admittance (common source) $V_{DS} = 10\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ y_{fs} $	>	2,5	4	6	7 mS
Feedback capacitance $V_{DS} = 10\text{ V}; V_{GS} = 0$ $V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	$C_{rs}$	typ.	0,3	0,3	—	— pF
	$C_{rs}$	typ.	—	—	0,3	0,3 pF
Noise figure at optimum source admittance $G_S = 1\text{ mS}; -B_S = 3\text{ mS}; f = 100\text{ MHz}$ Hz	F	typ.	1,5	1,5	—	— dB
		typ.	—	—	1,5	1,5 dB

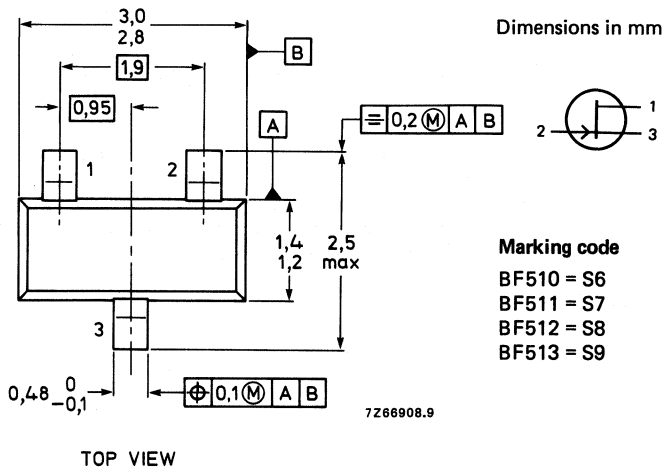
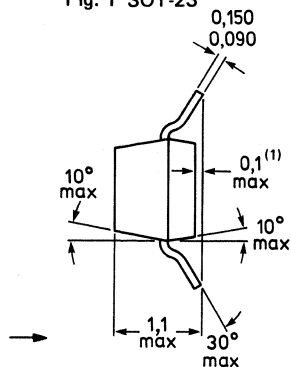
### MECHANICAL DATA

SOT-23.

See also *Soldering recommendations*.

**MECHANICAL DATA**

Fig. 1 SOT-23



**Marking code**

- BF510 = S6
- BF511 = S7
- BF512 = S8
- BF513 = S9

7Z66908.9

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 4

$V_{DS}$  max. 20 V

Drain-gate voltage (open source) see Fig. 4

$V_{DGO}$  max. 20 V

Drain current (d.c. or average)

$I_D$  max. 30 mA

Gate current

$\pm I_G$  max. 10 mA

Total power dissipation up to  $T_{amb} = 60\text{ }^\circ\text{C}^{**}$

$P_{tot}$  max. 250 mW

Storage temperature

$T_{stg}$  -65 to + 175  $^\circ\text{C}$

Junction temperature

$T_j$  max. 175  $^\circ\text{C}$

**THERMAL CHARACTERISTICS\***

$$T_j = P \times (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$$

**Thermal resistance**

From junction to tab

$R_{th\ j-t} = 60\text{ K/W}$

From tab to soldering points

$R_{th\ t-s} = 280\text{ K/W}$

From soldering points to ambient\*\*

$R_{th\ s-a} = 90\text{ K/W}$

\* See Thermal characteristics.

\*\* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$

			BF510	511	512	513
Gate cut-off current $-V_{GS} = 0,2\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	10	10	10	10 nA
Gate-drain breakdown voltage $I_S = 0; -I_D = 10\text{ }\mu\text{A}$	$-V_{(BR)GDO}$	>	20	20	20	20 V
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	0,7	2,5	6	10 mA
		<	3,0	7,0	12	18 mA
Gate-source cut-off voltage $I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3 V

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$  for BF510 and BF511

$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$  for BF512 and BF513

**y-parameters (common source)**

			BF510	511	512	513
Input capacitance at $f = 1\text{ MHz}$	$C_{is}$	<	5	5	5	5 pF
Input conductance at $f = 100\text{ MHz}$	$g_{is}$	typ.	100	90	60	50 $\mu\text{S}$
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	typ.	0,3	0,3	0,3	0,3 pF
		<	0,4	0,4	0,4	0,4 pF
Transfer admittance at $f = 1\text{ kHz}$ $V_{GS} = 0$ instead of $I_D = 5\text{ mA}$	$ y_{fs} $	>	2,5	4,0	4,0	3,5 mS
		>	—	—	6,0	7,0 mS
Transfer admittance at $f = 100\text{ MHz}$	$ y_{fs} $	typ.	3,5	5,5	5,0	5,0 mS
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	<	3	3	3	3 pF
Output conductance at $f = 1\text{ MHz}$	$g_{os}$	<	60	80	100	120 $\mu\text{S}$
Output conductance at $f = 100\text{ MHz}$	$g_{os}$	typ.	35	55	70	90 $\mu\text{S}$
Noise figure at optimum source admittance $G_S = 1\text{ mS}; -B_S = 3\text{ mS};$ $f = 100\text{ MHz}$	F	typ.	1,5	1,5	1,5	1,5 dB

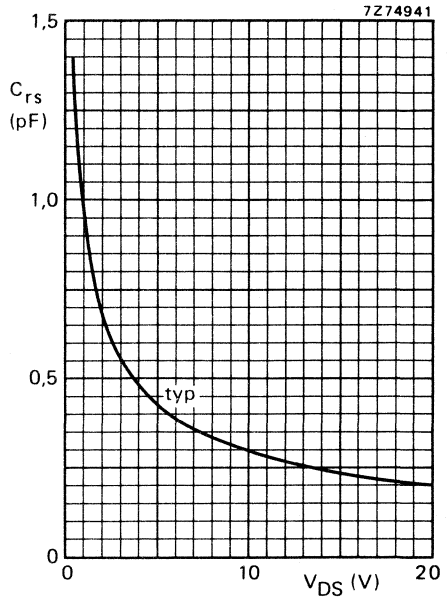


Fig. 2  $V_{GS} = 0$  for BF510 and BF511;  
 $I_D = 5$  mA for BF512 and BF513;  
 $f = 1$  MHz;  $T_{amb} = 25$  °C.

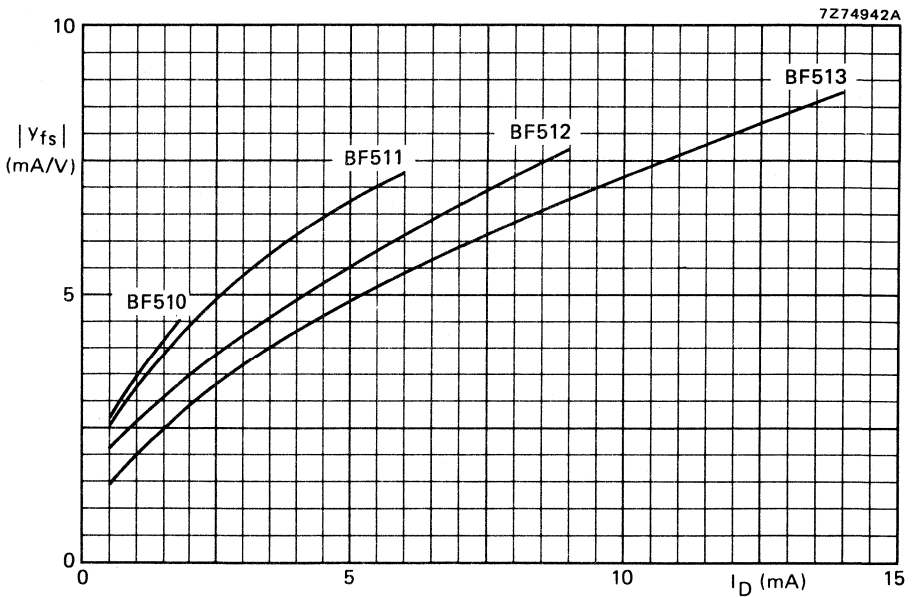


Fig. 3  $V_{DS} = 10$  V;  $f = 1$  kHz;  $T_{amb} = 25$  °C; typical values.



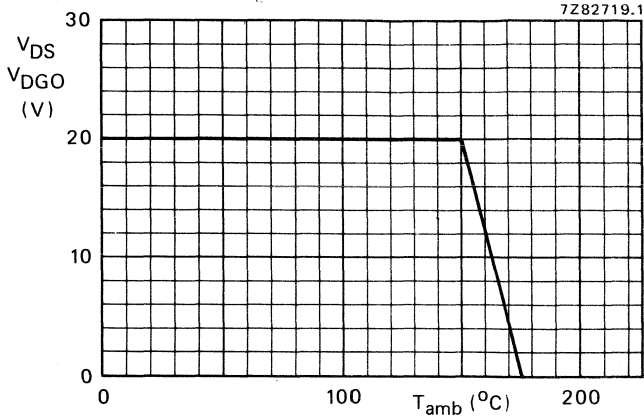


Fig. 4 Voltage derating curve.

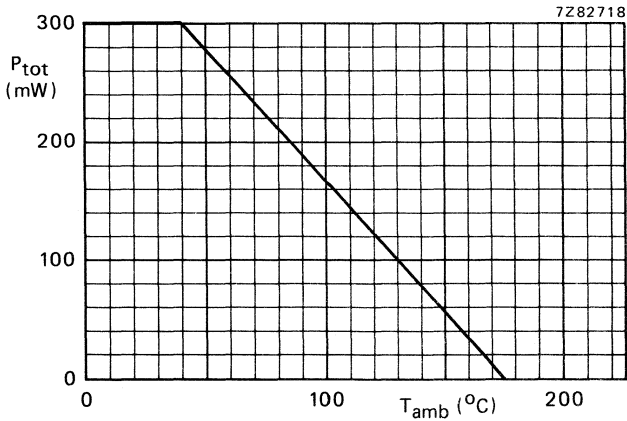


Fig. 5 Power derating curve.



## DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

## QUICK REFERENCE DATA

Characteristics measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $I_D = 200\text{ }\mu\text{A}$ ;  $V_{DG} = 15\text{ V}$

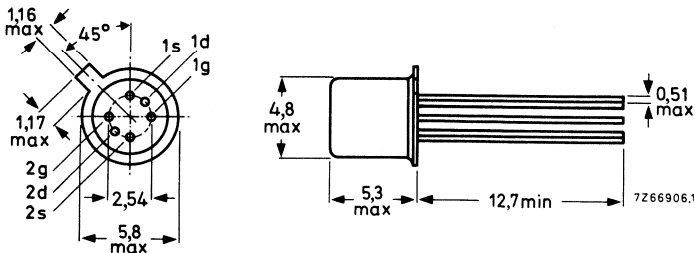
		BFQ10	11	12	13	14	15	16	
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left  \frac{d\Delta V_{GS}}{dT} \right $	< 5	5	10	20	20	40	50	$\mu\text{V/K}$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0,98	0,98	0,98	0,98	0,98	0,95	0,95	
	$\frac{g_{2fs}}{g_{1fs}}$	< 1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance	$\left  \Delta \frac{1}{g_{fs}} \right $	< 6	6	12	12	12	20	30	$\Omega$
Difference in penetration factor	$\left  \Delta \frac{g_{os}}{g_{fs}} \right $	< 10	30	30	30	30	30	100	$\mu\text{V/V}$
Common mode rejection ratio	CMRR	> 100	90	90	90	90	90	80	dB

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-71.

All leads insulated from the case.



**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V

Currents

Drain current	$I_D$	max.	30	mA
Gate current	$I_G$	max.	10	mA

Power dissipation

Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	250	mW
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Temperatures

Storage temperature	$T_{stg}$	-65 to +200	$^\circ\text{C}$
Junction temperature	$T_j$	max. 200	$^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	$^\circ\text{C}/\text{mW}$
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**CHARACTERISTICS** (total device) $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specifiedMeasured at:  $I_D = 200\text{ }\mu\text{A}$ ;  $V_{DG} = 15\text{ V}$  except for drain current ratio.

		BFQ10	11	12	13	14	15	16	
<u>Drain current ratio</u> 1)									
$V_{DG} = 15\text{ V}$ ; $V_{GS} = 0$	$\frac{I_{1D-1SS}}{I_{2D-2SS}}$	$> 0,97$ $< 1,03$	0,95 1,05	0,95 1,05	0,95 1,05	0,92 1,08	0,90 1,10	0,80 1,20	
<u>Difference in gate current</u>	$ \Delta I_G $	$< 10$	10	10	10	10	10	10	pA
<u>Gate-source voltage difference</u>	$ \Delta V_{GS} $	$< 5$	10	10	10	15	20	50	mV
<u>Thermal drift of gate-source voltage difference</u>	$\left  \frac{d \Delta V_{GS}}{dT} \right $	$< 5$	5	10	20	20	40	50	$\mu\text{V}/^{\circ}\text{C}$
<u>Transfer conductance ratio</u>	$\frac{g_{1fs}}{g_{2fs}}$	$> 0,98$ $< 1,02$	0,98 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,95 1,05	0,95 1,05	
<u>Difference in transfer impedance</u> 2)	$\left  \Delta \frac{1}{g_{fs}} \right $	$< 6$	6	12	12	12	20	30	$\Omega$
<u>Difference in penetration factor</u> 3)	$\left  \Delta \frac{g_{os}}{g_{fs}} \right $	$< 10$	30	30	30	30	30	100	$\mu\text{V}/\text{V}$
<u>Common mode rejection ratio</u> 4)	CMRR	$> 100$	90	90	90	90	90	80	dB

1) Measured under pulse conditions.

2) The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left( \Delta \frac{1}{g_{fs}} = \frac{d \Delta V_{GS}}{d I_D} \text{ at } V_{DG} = \text{constant} \right)$$

3) The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left( \Delta \frac{g_{os}}{g_{fs}} = \frac{d \Delta V_{GS}}{d V_{DG}} \text{ at } I_D = \text{constant} \right)$$

4) Common mode rejection ratio

$$\text{CMRR (in dB)} = -20 \log \left| \Delta \frac{g_{os}}{g_{fs}} \right|$$

## CHARACTERISTICS (Individual transistor)

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

### Gate cut-off current

$$-V_{GS} = 20\text{ V}; V_{DS} = 0$$

$$-I_{GSS} < 100\text{ pA}$$

$$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 125\text{ }^{\circ}\text{C}$$

$$-I_{GSS} < 20\text{ nA}$$

### Gate current

$$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}; T_{amb} = 125\text{ }^{\circ}\text{C}$$

$$I_G < 10\text{ nA}$$

### Drain current

$$V_{DS} = 15\text{ V}; V_{GS} = 0$$

$$I_{DSS} \quad 0,5\text{ to }10\text{ mA } ^1)$$

### Gate-source voltage

$$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$$

$$-V_{GS} < 2,7\text{ V}$$

### Gate-source cut-off voltage

$$I_D = 1\text{ nA}; V_{DG} = 15\text{ V}$$

$$-V_{(P)GS} \quad 0,5\text{ to }3,5\text{ V}$$

### Transfer conductance at $f = 1\text{ kHz}$

$$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$$

$$g_{fs} > 1,0\text{ mA/V}$$

### Output conductance at $f = 1\text{ kHz}$

$$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$$

$$g_{os} < 5\text{ }\mu\text{A/V}$$

### Input capacitance at $f = 1\text{ MHz}$

$$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$$

$$C_{is} < 8\text{ pF } ^2)$$

### Feedback capacitance at $f = 1\text{ MHz}$

$$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$$

$$C_{rs} < 1,0\text{ pF } ^2)$$

### Equivalent noise voltage

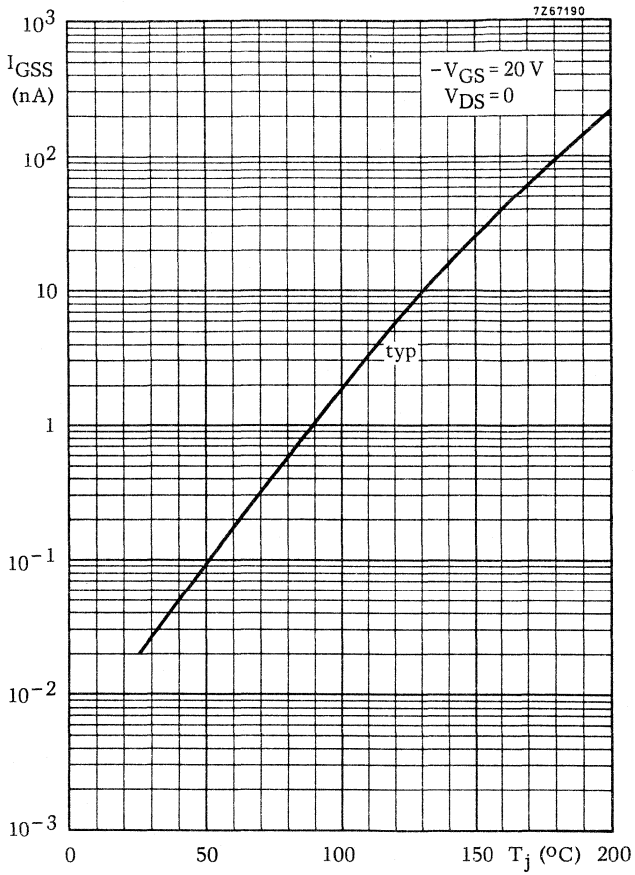
$$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$$

$$B = 0,6\text{ to }100\text{ Hz}$$

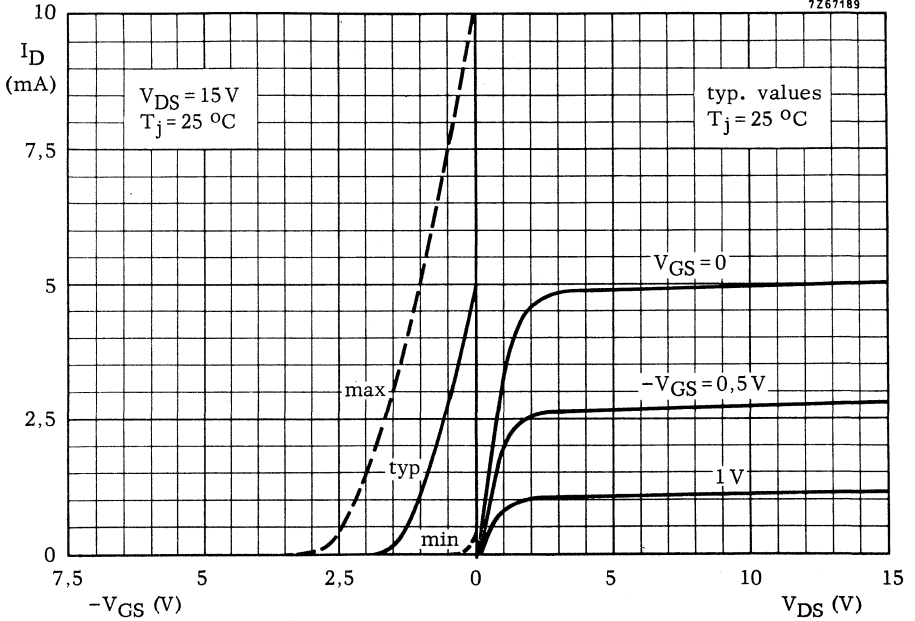
$$V_n < 0,5\text{ }\mu\text{V}$$

1) Measured under pulse conditions.

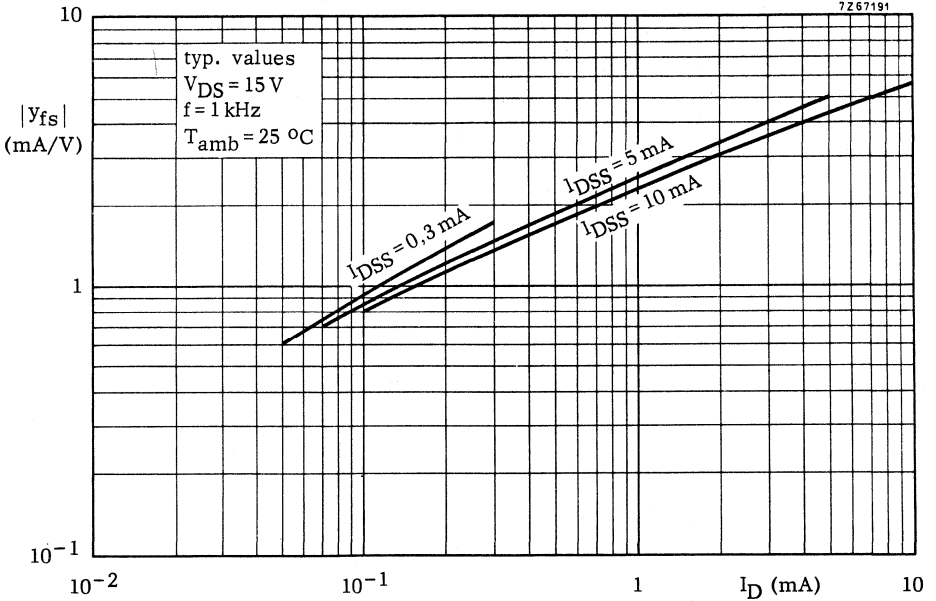
2) Measured with case grounded.



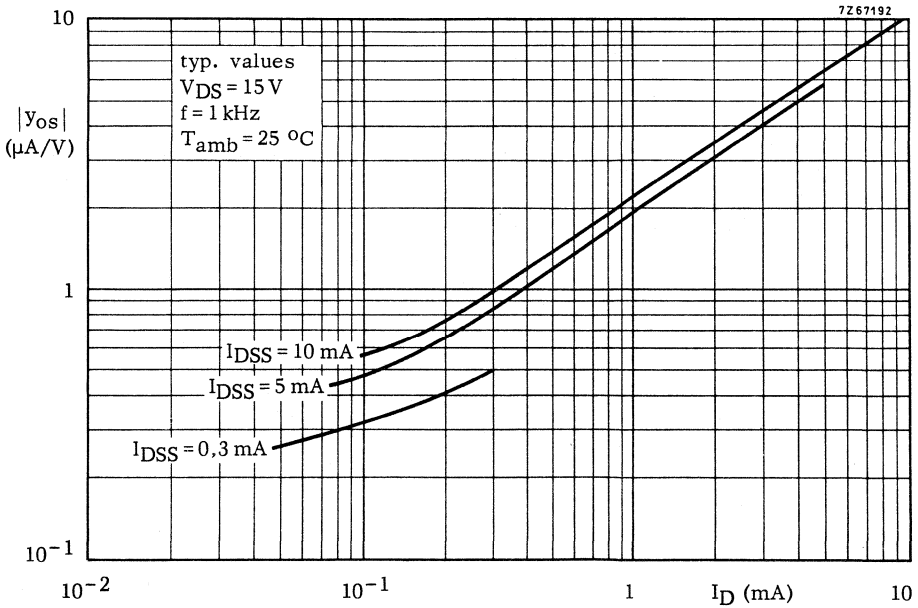
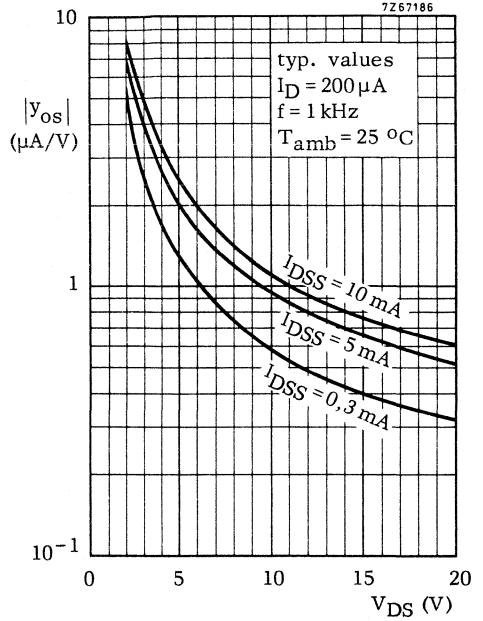
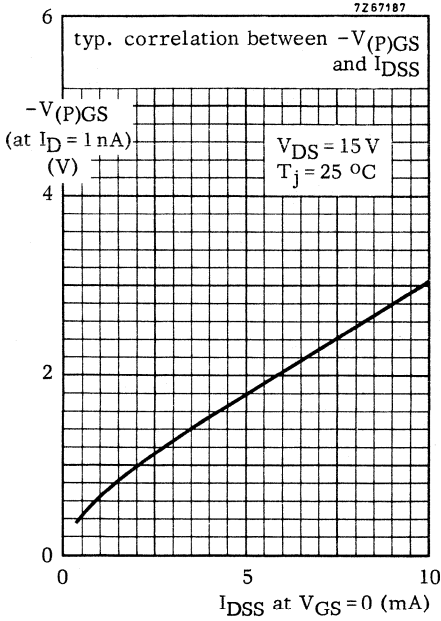
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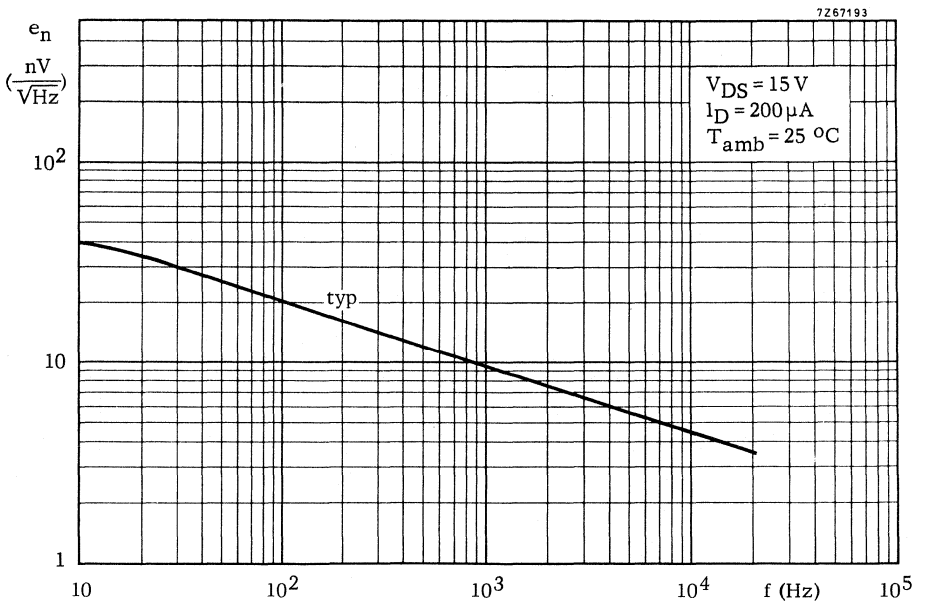
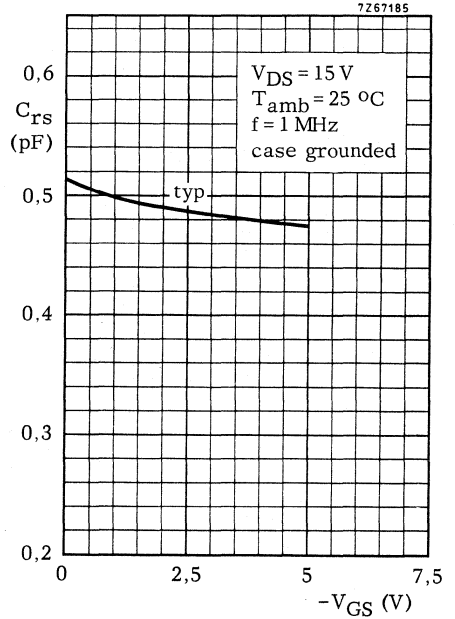
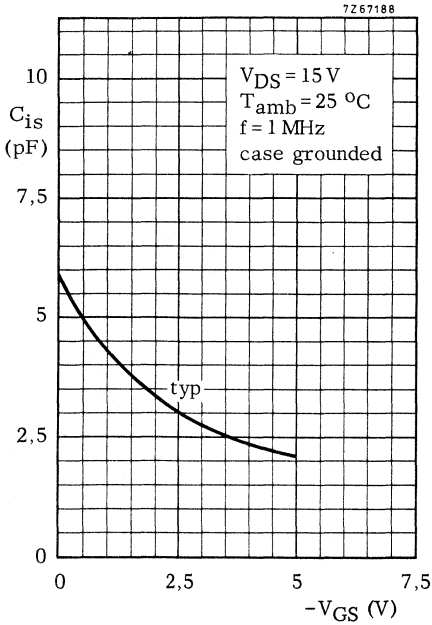


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## N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

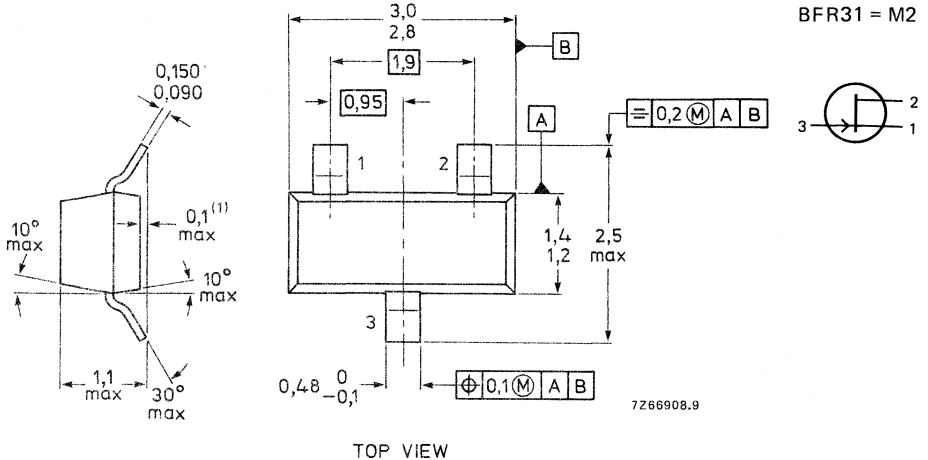
Planar epitaxial junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$ max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$ max.	25	V
Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	$P_{tot}$ max.	250	mW
		<b>BFR30</b>	<b>BFR31</b>
Drain current	$I_{DSS} >$	4	1 mA
$V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS} <$	10	5 mA
Transfer admittance (common source)	$ y_{fs}  >$	1,0	1,5 mS
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}; f = 1\text{ kHz}$	$ y_{fs}  <$	4,0	4,5 mS

### MECHANICAL DATA

Fig. 1 SOT-23.



(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 2	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source) see Fig. 2	$V_{DGO}$	max.	25	V
Gate-source voltage (open drain) see Fig. 2	$-V_{GSO}$	max.	25	V
Drain current	$I_D$	max.	10	mA
Gate current	$I_G$	max.	5	mA
Total power dissipation up to $T_{amb} = 65\text{ }^\circ\text{C}^{**}$	$P_{tot}$	max.	250	mW
Storage temperature	$T_{stg}$		-65 to + 175	$^\circ\text{C}$
Junction temperature	$T_j$	max.	175	$^\circ\text{C}$

**THERMAL CHARACTERISTICS\***

$$T_j = P \times (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$$

**Thermal resistance**

From junction to tab	$R_{th\ j-t}$	=	60	K/W
From tab to soldering points	$R_{th\ t-s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s-a}$	=	90	K/W

**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

			BFR30	BFR31	
Gate cut-off current					
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,2	0,2	nA
Drain current					
$V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	4	1	mA
		<	10	5	mA
Gate-source voltage					
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$	$-V_{GS}$	>	0,7	0	V
		<	3,0	1,3	V
$I_D = 50\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{GS}$	<	4,0	2,0	V
Gate-source cut-off voltage					
$I_D = 0,5\text{ nA}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	<	5	2,5	V

→ **y parameters**

Transfer admittance at $f = 1\text{ kHz}; T_{amb} = 25\text{ }^\circ\text{C}$					
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$	$ Y_{fs} $	>	1,0	1,5	mS
		<	4,0	4,5	mS
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$ Y_{fs} $	>	0,5	0,75	mS
Output admittance at $f = 1\text{ kHz}$					
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$	$ Y_{os} $	<	40	25	$\mu\text{S}$
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$ Y_{os} $	<	20	15	$\mu\text{S}$

\* See Thermal characteristics.

\*\* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

y parameters (continued)

Input capacitance at  $f = 1 \text{ MHz}$

$I_D = 1 \text{ mA}; V_{DS} = 10 \text{ V}$

$I_D = 200 \mu\text{A}; V_{DS} = 10 \text{ V}$

Feedback capacitance at  $f = 1 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

$I_D = 1 \text{ mA}; V_{DS} = 10 \text{ V}$

$I_D = 200 \mu\text{A}; V_{DS} = 10 \text{ V}$

Equivalent noise voltage

$I_D = 200 \mu\text{A}; V_{DS} = 10 \text{ V}$

$B = 0,6 \text{ to } 100 \text{ Hz}$

		BFR30	BFR31	
$C_{is}$	<	4	4	pF
$C_{is}$	<	4	4	pF
$C_{rs}$	<	1,5	1,5	pF
$C_{rs}$	<	1,5	1,5	pF
$V_n$	<	0,5	0,5	$\mu\text{V}$

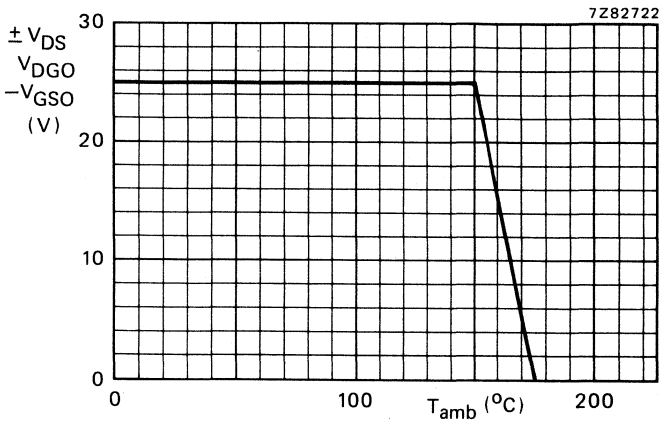


Fig. 2 Voltage derating curve.

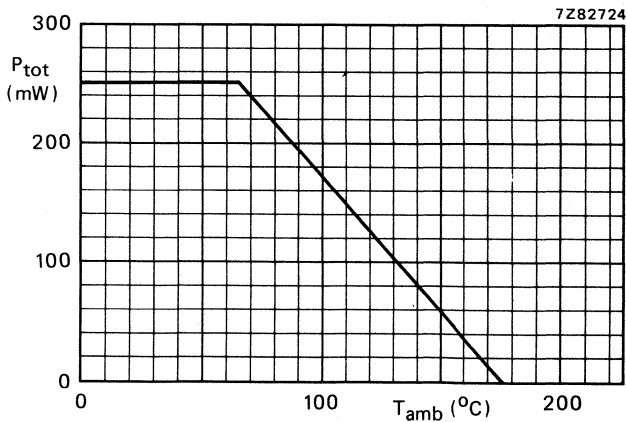


Fig. 3 Power derating curve.

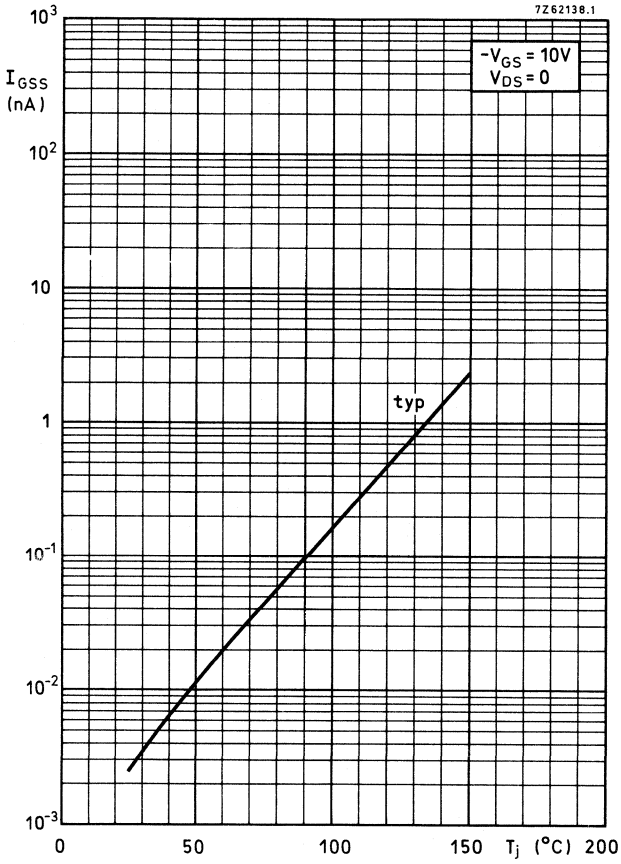


Fig. 4.

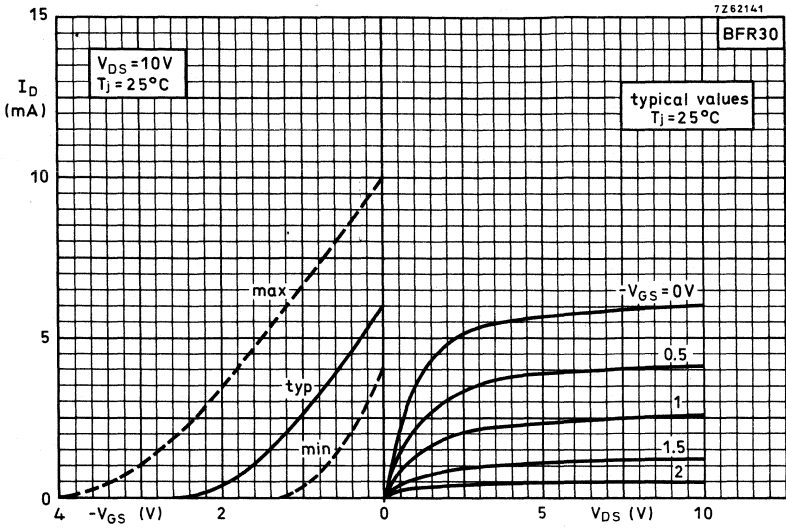


Fig. 5.

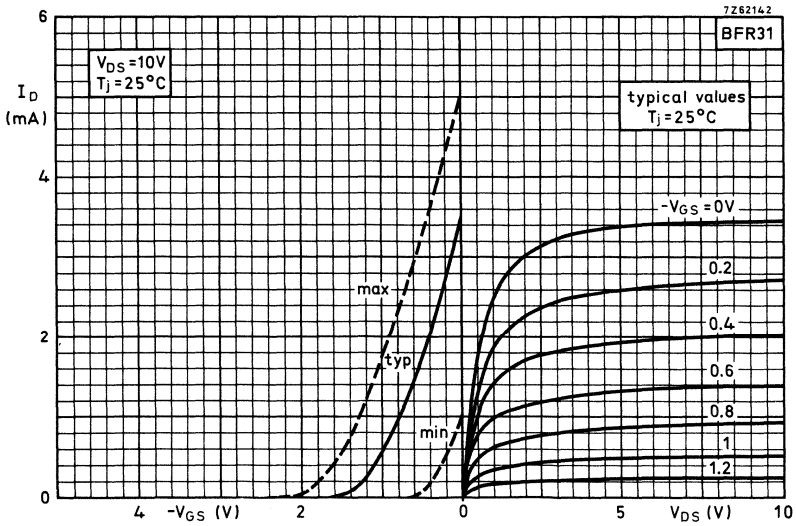


Fig. 6.

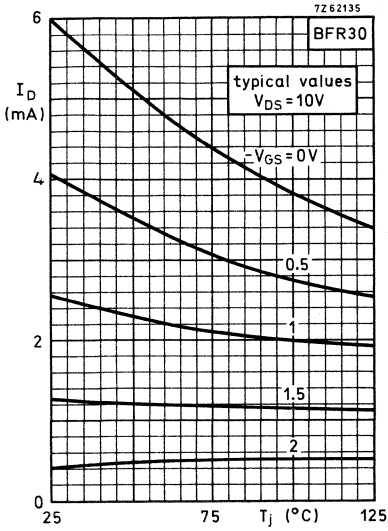


Fig. 7.

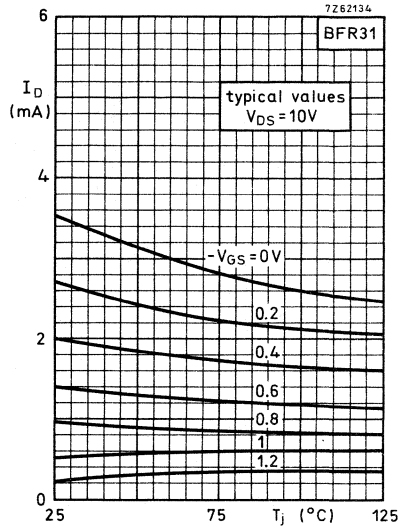


Fig. 8.

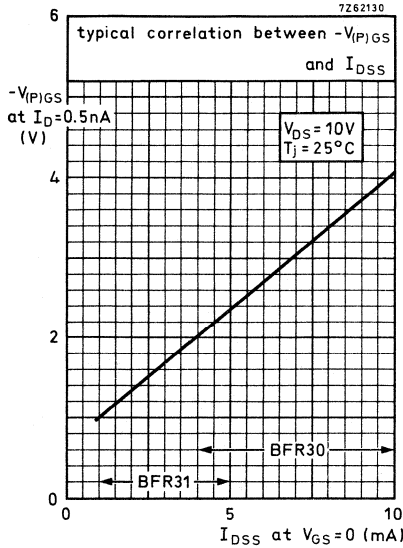


Fig. 9.



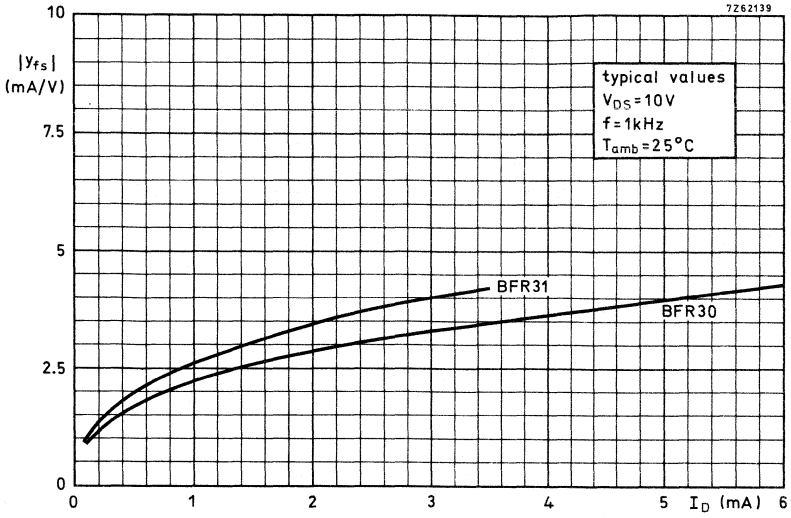


Fig. 10.

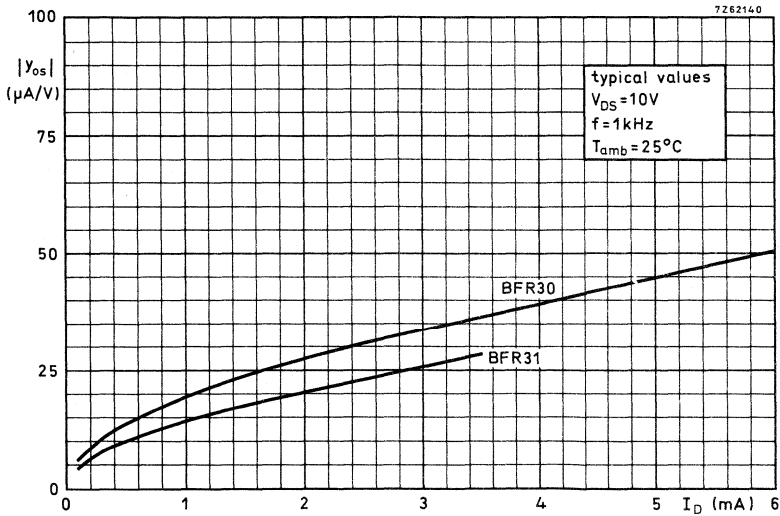


Fig. 11.

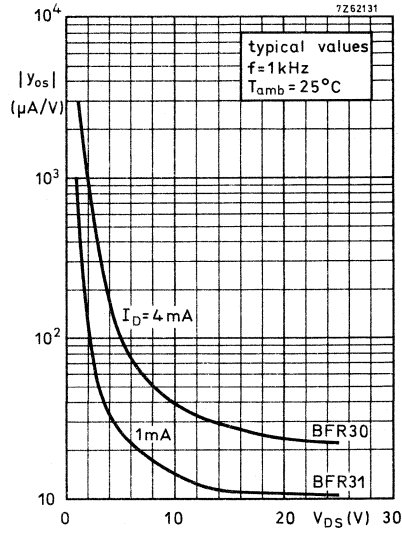


Fig. 12.

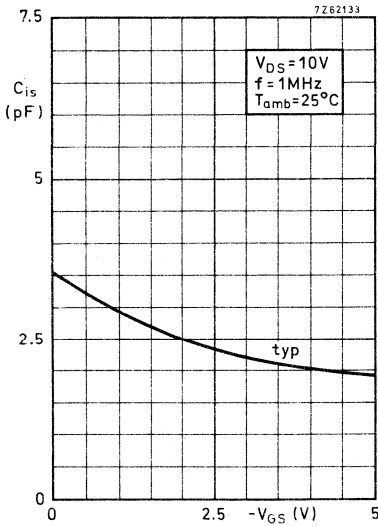


Fig. 13.

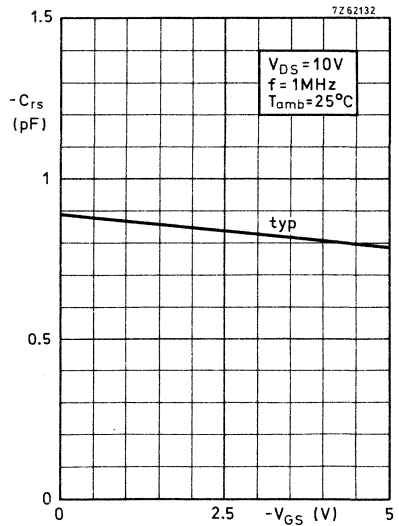


Fig. 14.

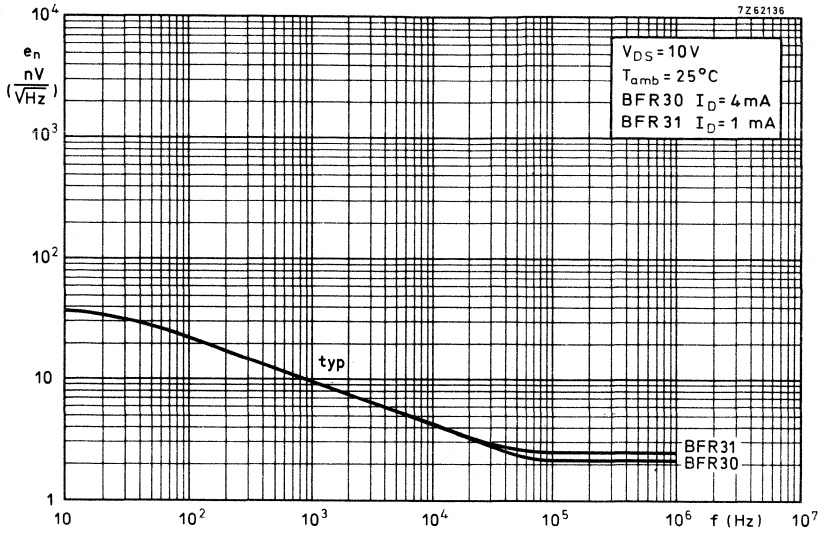


Fig. 15.

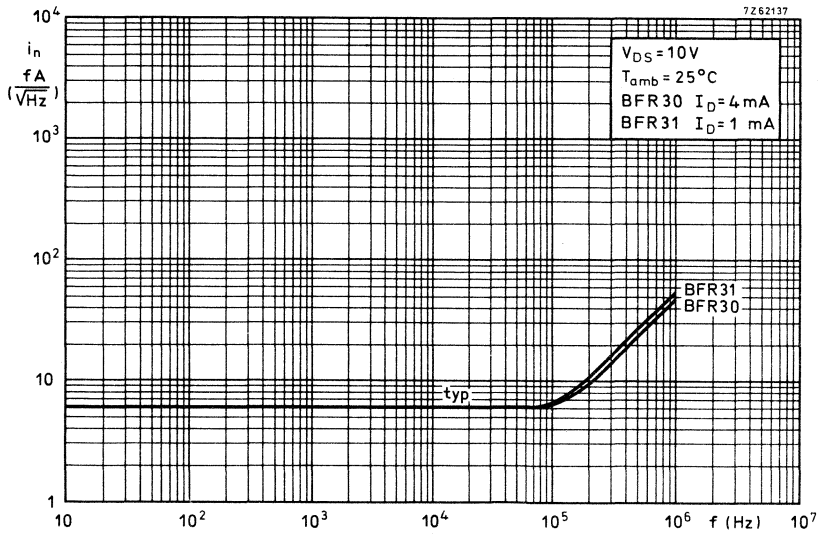


Fig. 16.



## N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

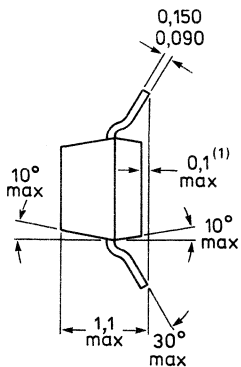
Symmetrical n-channel silicon junction field-effect transistor, designed primarily for use as a source follower with the input protected against successive voltage surges by a forward and reverse integrated diode.

### QUICK REFERENCE DATA

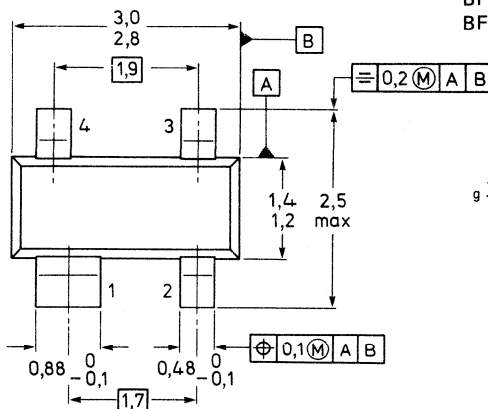
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	30 V
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	200 mW
Drain current			
$V_{DS} = 6\text{ V}; V_{GS} = 0$ : BFR101A	$I_{DSS}$	0,2 to 1,5 mA	
$V_{DS} = 6\text{ V}; V_{GS} = 0$ : BFR101B	$I_{DSS}$	1,0 to 5,0 mA	
Transfer admittance (common source)			
$V_{DS} = 6\text{ V}; V_{GS} = 0$ ; $f = 1\text{ kHz}$ : BFR101A	$ Y_{fs} $	>	1,2 mS
$V_{DS} = 6\text{ V}; V_{GS} = 0$ ; $f = 1\text{ kHz}$ : BFR101B	$ Y_{fs} $	>	2,5 mS

### MECHANICAL DATA

Fig. 1 SOT-143.

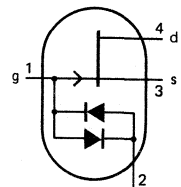


Dimensions in mm



### Marking code

BFR101A = M97  
BFR101B = M98



TOP VIEW

7Z85014.6

(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current (d.c.)	$I_D$	max.	20 mA
Gate current (d.c.)	$I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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**CHARACTERISTICS** with source connected to case for all measurements

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

		<b>BFR101A</b>	<b>BFR101B</b>
Gate leakage current $V_{DS} = 6\text{ V}; I_D = 10\text{ }\mu\text{A}$	$-I_G$	< 5	5 nA
Drain current* $V_{DS} = 6\text{ V}; V_{GS} = 0$	$I_{DSS}$	0,2 to 1,5	1 to 5 mA
Gate-source cut-off voltage $V_{DS} = 6\text{ V}; I_D = 1\text{ }\mu\text{A}$	$-V_{(P)GS}$	0,2 to 1	0,5 to 2,5 V
<b>Small-signal common-source characteristics</b> $V_{DS} = 6\text{ V}; V_{GS} = 0$			
Transfer admittance* $f = 1\text{ kHz}$	$ Y_{fs} $	> 1,2	2,5 mS
Output admittance at $f = 1\text{ kHz}^{**}$	$ Y_{os} $	typ. 10	50 mS
Input capacitance at $f = 1\text{ MHz}$ diodes not connected	$C_{is}$	< 5	5 pF
Diode capacitance $V_D = 0$ ; source and drain not connected	$C_d$	typ. 0,7	0,7 pF
Diode forward voltage $\pm I_F = 10\text{ mA}$	$V_F$	0,7 to 1,2	0,7 to 1,2 V

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

\*\* Measured under pulse conditions:  $t_p = 100\text{ ms}; \delta \leq 0,1$ .

## MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

### QUICK REFERENCE DATA

Characteristics measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $I_D = 0,5\text{ mA}$ ;  $V_{DG} = 15\text{ V}$

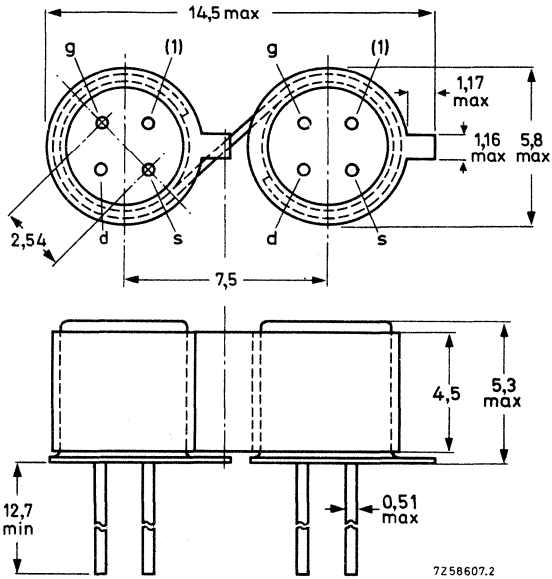
		BFS21	BFS21A
Gate cut-off current	$I_G$	< 0,5	0,5 nA
Gate -source voltage difference	$ \Delta V_{GS} $	< 20	10 mV
Thermal drift of gate-source voltage difference	$\left  \frac{d\Delta V_{GS}}{dT} \right $	< 75	40 $\mu\text{V/K}$
Difference in transfer impedance	$\left  \Delta \frac{1}{g_{fs}} \right $	< 15	7,5 $\Omega$
Difference in penetration factor	$\left  \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	0,5 mV/V
Common mode rejection ratio	CMRR	> 60	66 dB

### MECHANICAL DATA

SOT-52 (see next page)

TOTAL DEVICE  
MECHANICAL DATA  
SOT-52

Dimensions in mm



(1) = shield lead (connected to case).

Maximum lead diameter is guaranteed only for 12,7 mm.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	$I_D$	max.	4 mA
Gate current	$I_G$	max.	0,5 mA
Total power dissipation up to $T_{amb} = 100\text{ }^\circ\text{C}$	$P_{tot}$	max.	30 mW
Operating ambient temperature	$T_{amb}$		-20 to + 100 °C



**CHARACTERISTICS** (total device)

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

		BFS21	BFS21A
<u>Drain current ratio</u>			
$V_{DG} = 15\text{ V}; V_{GS} = 0; T_j = 25\text{ }^{\circ}\text{C}$	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	$> 0.95$ $< 1.05$	0.95 1.05
<u>Gate-source voltage difference</u>			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS} $	$< 20$	10 mV
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS} $	$< 20$	10 mV
<u>Thermal drift of gate-source voltage difference</u>			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left  \frac{d \Delta V_{GS}}{dT} \right $	$< 75$	40 $\mu\text{V}/^{\circ}\text{C}$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left  \frac{d \Delta V_{GS}}{dT} \right $	$< 75$	40 $\mu\text{V}/^{\circ}\text{C}$
<u>Change of gate-source voltage difference with ambient temperature</u>			
$T_{amb} = 25\text{ to }100\text{ }^{\circ}\text{C}$			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) $	$< 6$	3 mV
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) $	$< 6$	3 mV
<u>Difference of penetration factors <sup>1)</sup></u>			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left  \Delta \frac{g_{os}}{g_{fs}} \right $	$< 1$	0.5 $10^{-3}$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left  \Delta \frac{g_{os}}{g_{fs}} \right $	$< 1$	0.5 $10^{-3}$
<u>Difference of transfer impedances <sup>2)</sup></u>			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left  \Delta \frac{1}{g_{fs}} \right $	$< 15$	7.5 $\Omega$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left  \Delta \frac{1}{g_{fs}} \right $	$< 75$	37.5 $\Omega$

1) The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left( \Delta \frac{g_{os}}{g_{fs}} = \frac{d \Delta V_{GS}}{d V_{DG}} \text{ at } I_D = \text{constant} \right)$$

2) The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left( \Delta \frac{1}{g_{fs}} = \frac{d \Delta V_{GS}}{d I_D} \text{ at } V_{DG} = \text{constant} \right)$$

**CHARACTERISTICS** (continued) (total device)

Common mode rejection ratio <sup>1)</sup>

$I_D = 500 \mu A; V_{DG} = 15 V$

	BFS21	BFS21A
CMRR	> 60	66 dB
CMRR	> 60	66 dB

$I_D = 100 \mu A; V_{DG} = 15 V$

**INDIVIDUAL TRANSISTOR**

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage

$\pm V_{DS}$  max. 30 V

Drain-gate voltage (open source)

$V_{DGO}$  max. 30 V

Gate-source voltage (open drain)

$-V_{GSO}$  max. 30 V

Currents

Drain current

$I_D$  max. 20 mA

Gate current

$I_G$  max. 10 mA

Power dissipation

Total power dissipation up to  $T_{amb} = 25^\circ$

$P_{tot}$  max. 300 mW

Temperatures

Storage temperature

$T_{stg}$   $-65$  to  $+200$   $^\circ C$

Junction temperature

$T_j$  max. 200  $^\circ C$

**THERMAL RESISTANCE**

From junction to ambient in free air  
(for individual transistor without S-clip)

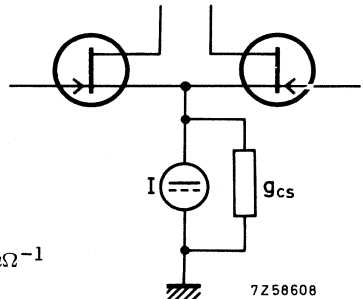
$R_{th j-a} = 0.59$   $^\circ C/mW$

<sup>1)</sup> Common mode rejection ratio

$$(CMRR)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \frac{1}{2} g_{cs} \Delta \frac{1}{g_{fs}}$$

where  $g_{cs}$  in this formula is the output conductance of the summing current source.

The guaranteed values of CMRR apply at  $g_{cs} = 0.1 \mu\Omega^{-1}$



**CHARACTERISTICS** (individual transistor)  $T_{amb} = 25^{\circ}\text{C}$  unless otherwise specified

Gate cut-off current

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$   $I_G < 0.5 \text{ nA}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}; T_{amb} = 100^{\circ}\text{C}$   $I_G < 25 \text{ nA}$

Drain current

$V_{DS} = 15 \text{ V}, V_{GS} = 0, T_j = 25^{\circ}\text{C}$   $I_{DSS} > 1 \text{ mA}$

Gate-source cut-off voltage

$I_D = 0.5 \text{ nA}, V_{DS} = 15 \text{ V}$   $-V_{(P)GS} < 6 \text{ V}$

Transfer conductance at  $f = 1 \text{ kHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$   $g_{fs} > 1.0 \text{ m}\Omega^{-1}$

Output conductance at  $f = 1 \text{ kHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$   $g_{os} < 15 \mu\Omega^{-1}$

Input capacitance at  $f = 1 \text{ MHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$   $C_{is} < 5 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$   $C_{rs} < 0.75 \text{ pF}$

Equivalent noise voltage

$f = 10 \text{ Hz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$   $V_n/\sqrt{B} < 200 \text{ nV}/\sqrt{\text{Hz}}$

$V_{DS} = 15 \text{ V}, V_{GS} = 0$   $V_n/\sqrt{B} < 75 \text{ nV}/\sqrt{\text{Hz}}$



## N-CHANNEL SILICON FET

N-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	250 mW
Drain current			
$V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	0,2 mA
		<	1,5 mA
Transfer admittance (common source)			
$I_D = 0,2\text{ mA}; V_{DS} = 10\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	>	0,5 mS
Equivalent noise voltage			
$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A}; B = 0,6\text{ to }100\text{ Hz}$	$V_n$	<	0,5 $\mu\text{V}$

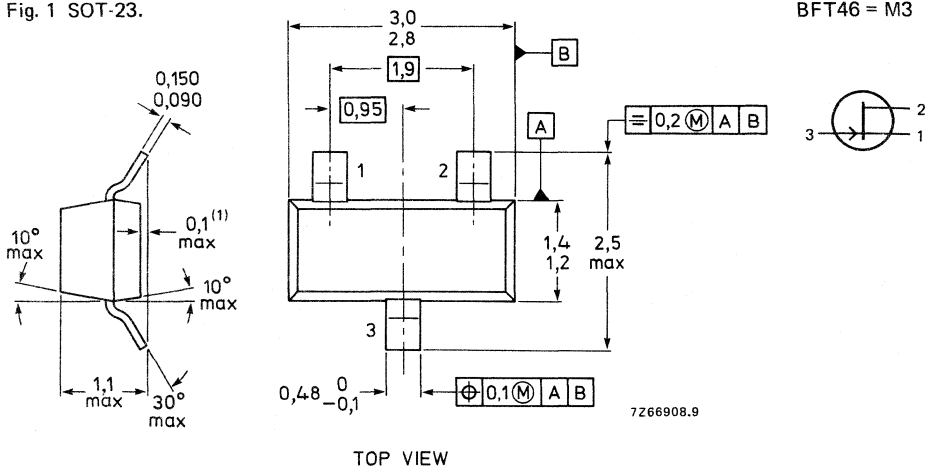
### MECHANICAL DATA

Dimensions in mm

Marking code

Fig. 1 SOT-23.

BFT46 = M3



(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	$I_D$	max.	10 mA
Gate current	$I_G$	max.	5 mA
Total power dissipation up to $T_{amb} = 65\text{ }^\circ\text{C}^{**}$	$P_{tot}$	max.	250 mW
Storage temperature	$T_{stg}$		-65 to +175 $^\circ\text{C}$
Junction temperature	$T_j$	max.	175 $^\circ\text{C}$

## THERMAL CHARACTERISTICS\*

$$R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a} = \frac{T_j - T_{amb}}{P}$$

### Thermal resistance

From junction to tab	$R_{th\ j-t}$	=	60 K/W
From tab to soldering points	$R_{th\ t-s}$	=	280 K/W
From soldering points to ambient**	$R_{th\ s-a}$	=	90 K/W

## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off current $-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,2 nA
Drain current ** $V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	0,2 mA
		<	1,5 mA
Gate-source voltage $I_D = 50\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{GS}$	>	0,1 V
		<	1,0 V
Gate-source cut-off voltage $I_D = 0,5\text{ nA}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	<	1,2 V

→ y-parameters at  $f = 1\text{ kHz}; V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}$

Transfer admittance	$ y_{fs} $	>	1,0 mS
Output admittance	$ y_{os} $	<	10 $\mu\text{S}$
$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A};$			
Transfer admittance	$ y_{fs} $	>	0,5 mS
Output admittance	$ y_{os} $	<	5 $\mu\text{S}$

\* See *Thermal characteristics*.

\*\* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at  $f = 1 \text{ MHz}$ ;

$V_{DS} = 10 \text{ V}$ ;  $V_{GS} = 0$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

$C_{is} < 5 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$ ;

$V_{DS} = 10 \text{ V}$ ;  $V_{GS} = 0$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

$C_{rs} < 1,5 \text{ pF}$

Equivalent noise voltage

$V_{DS} = 10 \text{ V}$ ;  $I_D = 200 \text{ } \mu\text{A}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

$B = 0,6 \text{ to } 100 \text{ Hz}$

$V_n < 0,5 \text{ } \mu\text{V}$

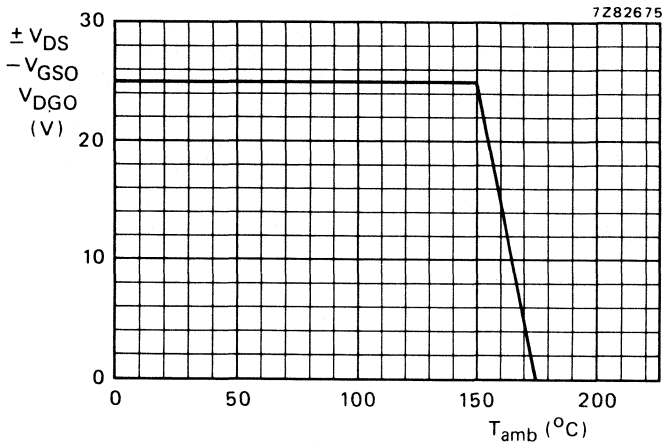


Fig. 2 Voltage derating curve.

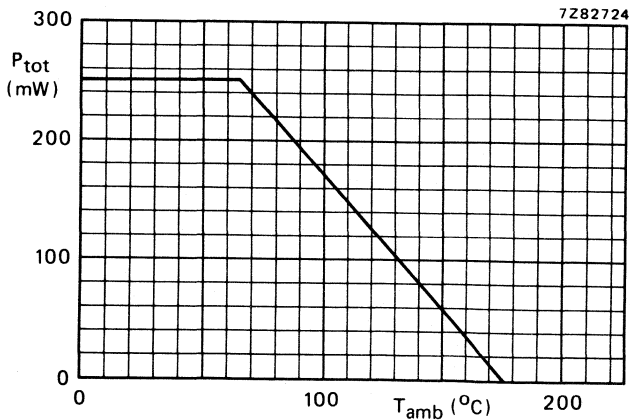


Fig. 3 Power derating curve.

7Z78216

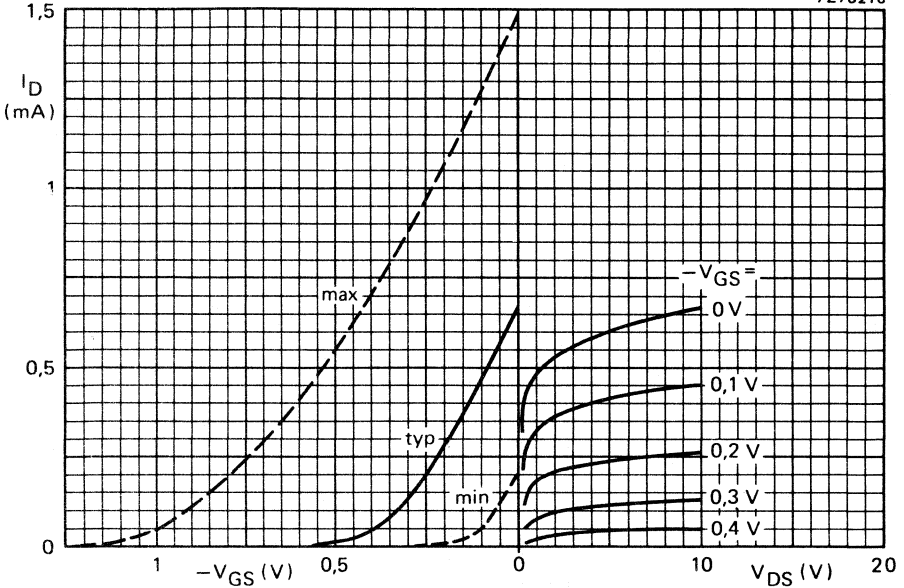


Fig. 4 Typical values.  $V_{DS} = 10V$ ;  $T_j = 25^\circ C$ .

7Z78214

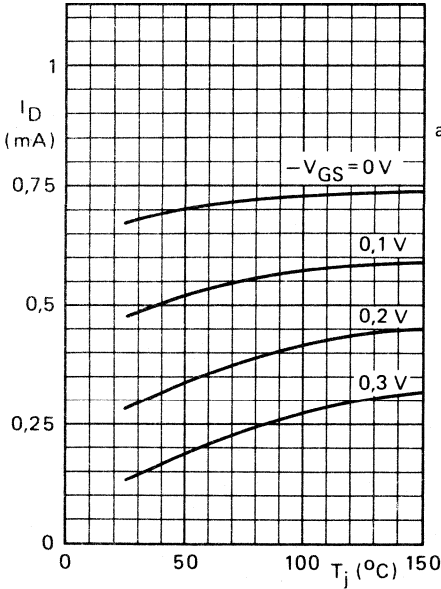


Fig. 5 Typical values.  $V_{DS} = 10V$ .

7Z77642

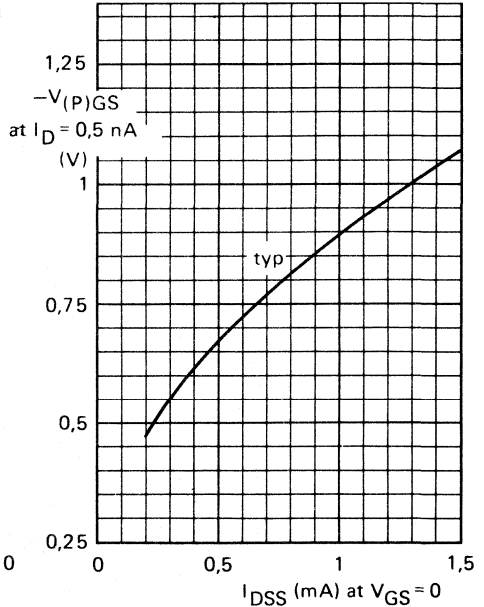


Fig. 6 Correlation between  $-V_{(P)GS}$  and  $I_{DSS}$ .  $V_{DS} = 10V$ ;  $T_j = 25^\circ C$ .



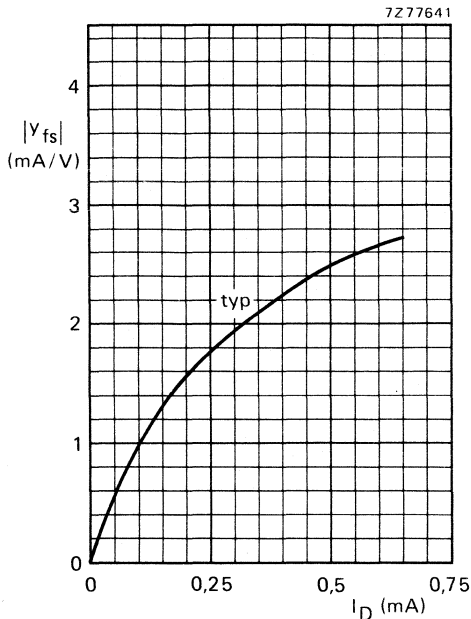


Fig. 7.

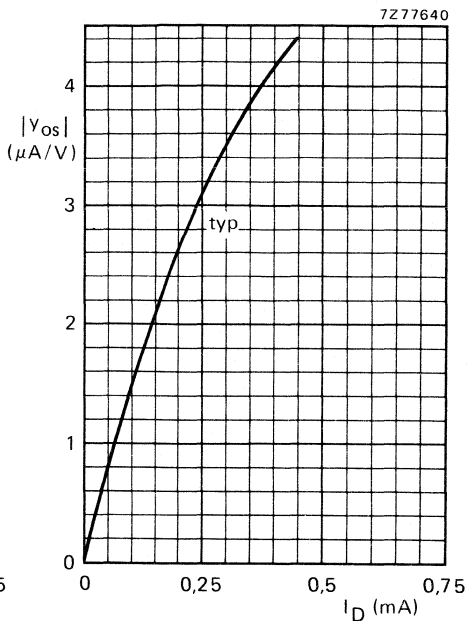


Fig. 8.

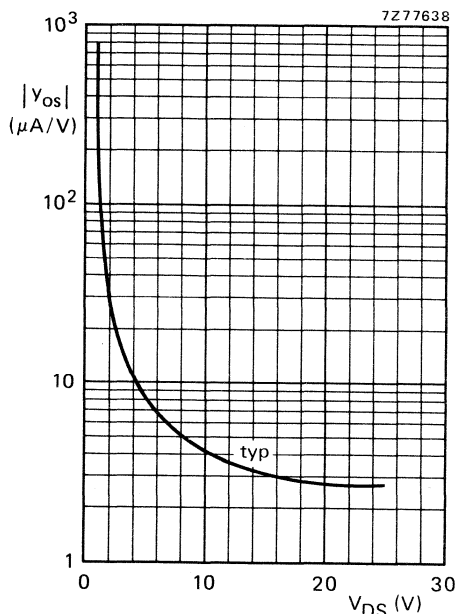


Fig. 9.

Fig. 7  $|Y_{fs}|$  versus  $I_D$ .  
 $V_{DS} = 10$  V;  $f = 1$  kHz;  $T_{amb} = 25$  °C.

Fig. 8  $|Y_{os}|$  versus  $I_D$ .  
 $V_{DS} = 10$  V;  $f = 1$  kHz;  $T_{amb} = 25$  °C.

Fig. 9  $|Y_{os}|$  versus  $V_{DS}$ .  
 $I_D = 0,4$  mA;  $f = 1$  kHz;  $T_{amb} = 25$  °C.

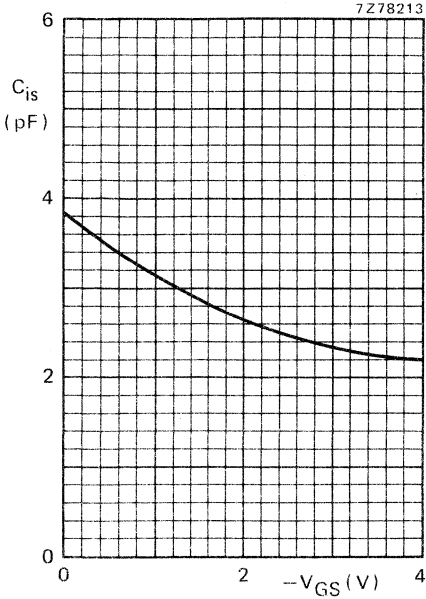


Fig. 10.

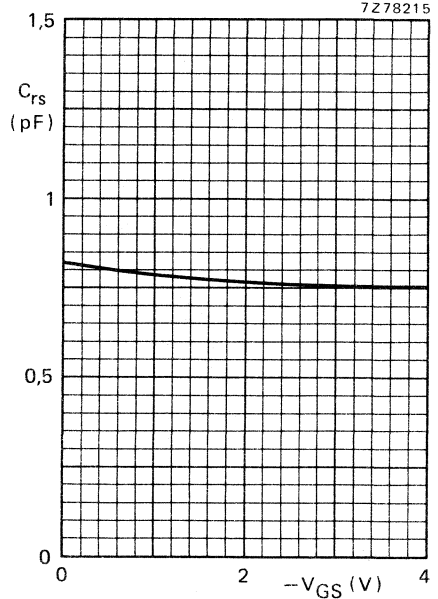


Fig. 11.

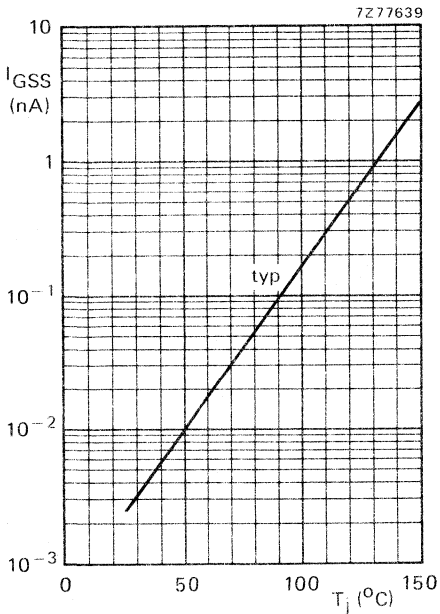


Fig. 12.

Fig.10 Typical values.  
 $V_{DS} = 10$  V,  $T_{amb} = 25$  °C.

Fig.11 Typical values.  
 $V_{DS} = 10$  V,  $T_{amb} = 25$  °C.

Fig.12  $I_{GSS}$  versus  $T_j$ .  
 $-V_{GSS} = 10$  V;  $V_{DS} = 0$ .

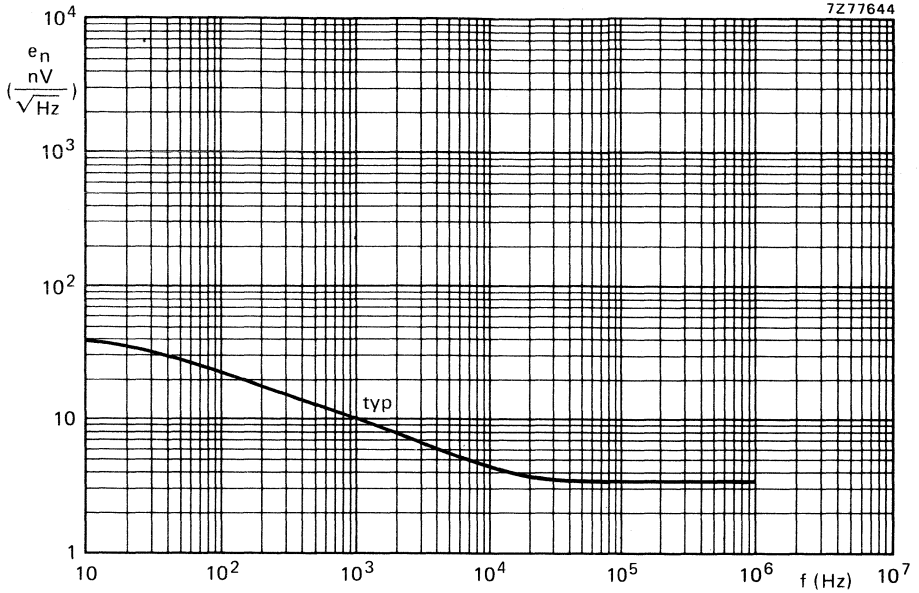


Fig. 13  $V_{DS} = 10 V$ ;  $I_D = 0,2 mA$ ;  $T_{amb} = 25 ^\circ C$ .

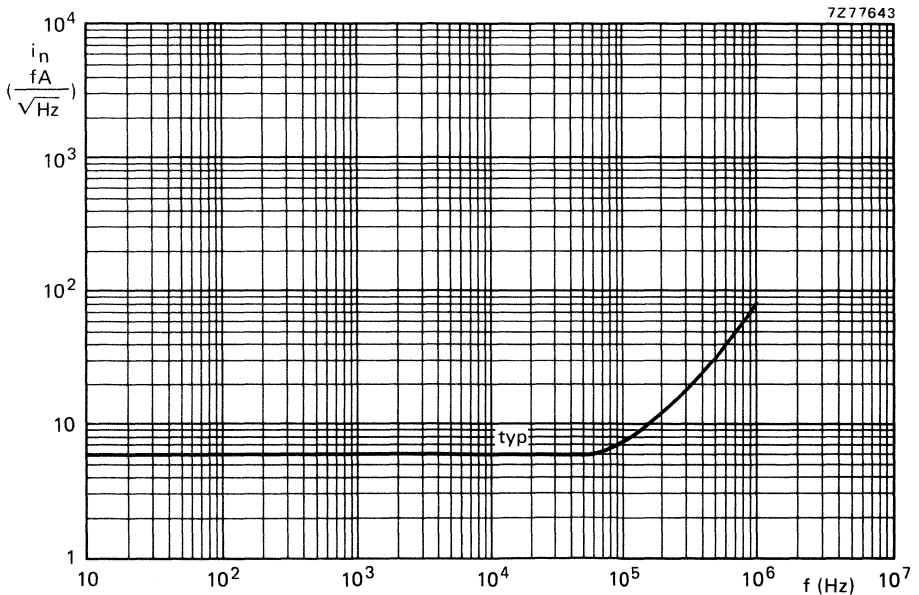


Fig. 14  $V_{DS} = 10 V$ ;  $I_D = 0,2 mA$ ;  $T_{amb} = 25 ^\circ C$ .



## N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

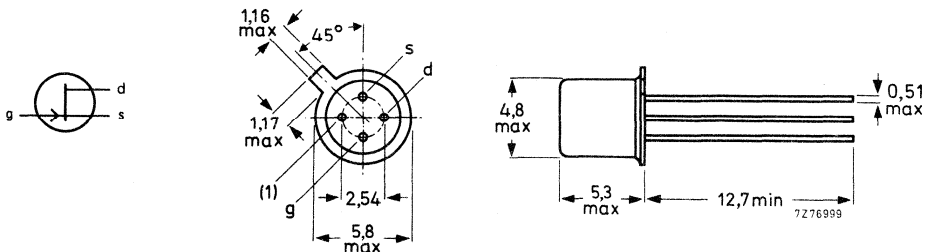
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300	mW
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	$>$	8	4 mA
		$<$	20	10 mA
Gate-source cut-off voltage $I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	$<$	8	6 V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	$C_{rs}$	$<$	0,80	0,80 pF
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 200\text{ MHz}$	$ Y_{fs} $	$>$	3,2	3,2 mS
Noise figure at $V_{DS} = 15\text{ V}; V_{GS} = 0$ $f = 100\text{ MHz}; R_G = 1\text{ k}\Omega$	F	$<$	2,5	2,5 dB
Equivalent noise voltage $f = 10\text{ Hz}$	$V_{n\sqrt{B}}$	$<$	75	75 $\text{nV}/\sqrt{\text{Hz}}$

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	$I_D$	max.	20 mA
Gate current	$I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
Storage temperature	$T_{stg}$		-65 to +200 $^\circ\text{C}$
Junction temperature	$T_j$	max.	200 $^\circ\text{C}$

**THERMAL RESISTANCE**

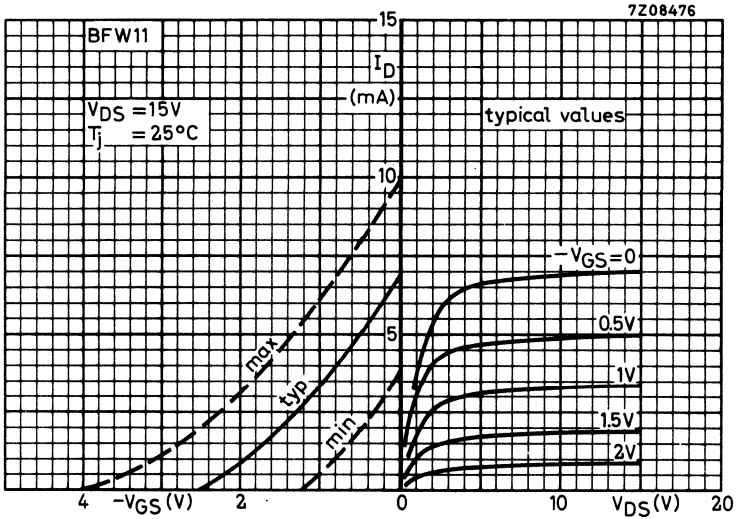
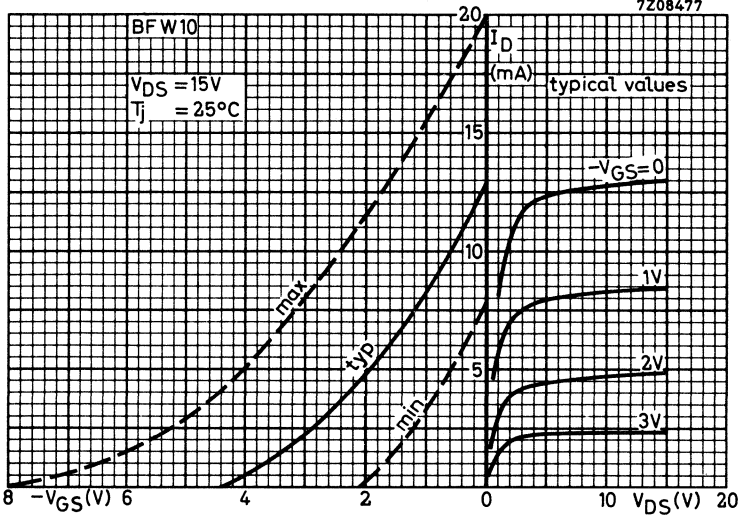
→ From junction to ambient  $R_{th\ j-a} = 0.59\text{ K/mW}$

## CHARACTERISTICS

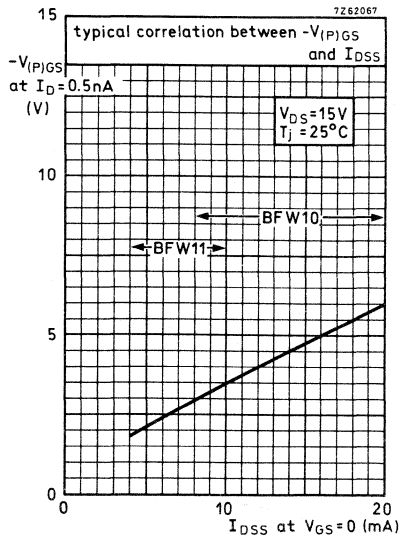
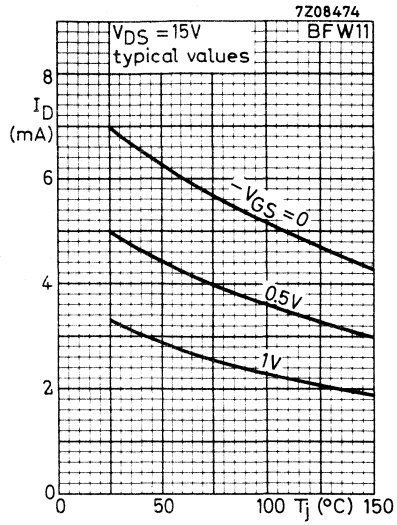
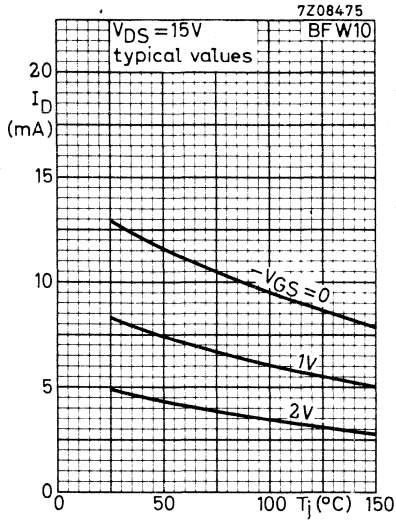
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off currents	BFW10		BFW11		
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	< 0.1	0.1	nA	
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 150\text{ }^\circ\text{C}$	$-I_{GSS}$	< 0.5	0.5	$\mu\text{A}$	
Drain current <sup>1)</sup>					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	> 8 < 20	4 10	mA mA	
Gate-source voltage					
$I_D = 400\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> 2.0 < 7.5	V V		
$I_D = 50\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> 1.25 < 4.0	V V		
Gate-source cut-off voltage					
$I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	< 8	6	V	
y parameters					
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}$					
$f = 1\text{ kHz}$ Transfer admittance	$ y_{fs} $	> 3.5 < 6.5	3.0 6.5	mS mS	←
Output admittance	$ y_{os} $	< 85	50	$\mu\text{S}$	←
$f = 1\text{ MHz}$ Input capacitance	$C_{is}$	typ. 4 < 5	4 5	pF pF	
Feedback capacitance	$-C_{rs}$	typ. 0.6 < 0.80	0.6 0.80	pF pF	
$f = 200\text{ MHz}$ Transfer admittance	$ y_{fs} $	> 3.2	3.2	mS	←
Input conductance	$g_{is}$	< 800	800	$\mu\text{S}$	
Output conductance	$g_{os}$	< 200	100	$\mu\text{S}$	←
Noise figure at $f = 100\text{ MHz}; R_G = 1\text{ k}\Omega$					
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}$ input tuned to minimum noise	F	< 2.5	2.5	dB	
Equivalent noise voltage					
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}$ $f = 10\text{ Hz}$	$V_n/\sqrt{B}$	< 75	75	nV/ $\sqrt{\text{Hz}}$	

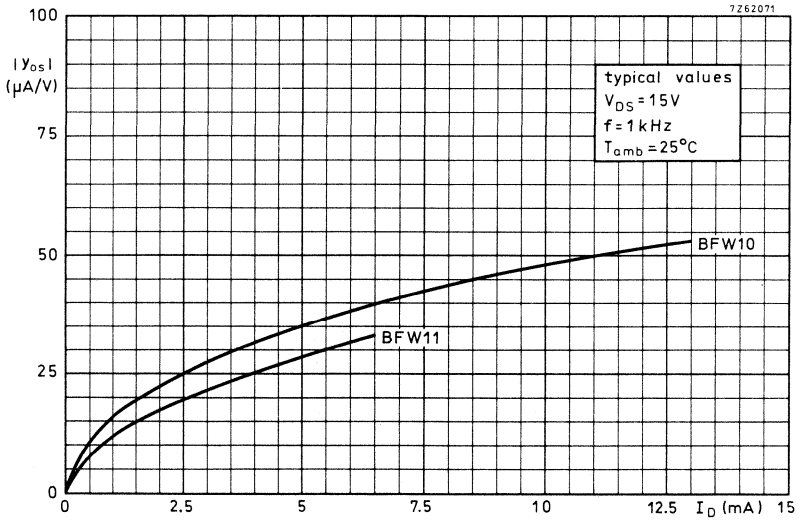
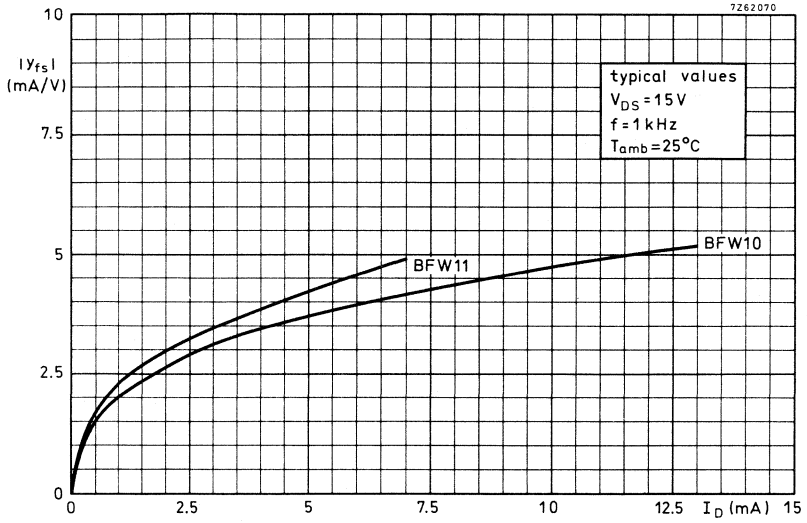
<sup>1)</sup> Measured under pulsed conditions.

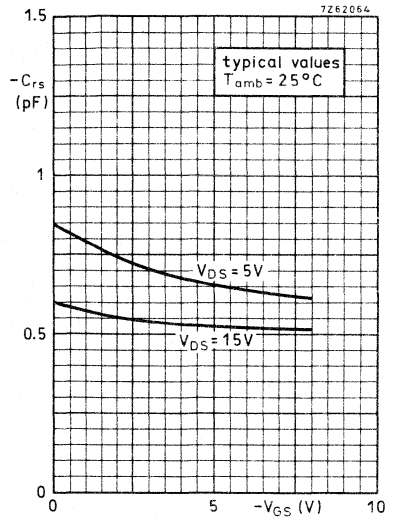
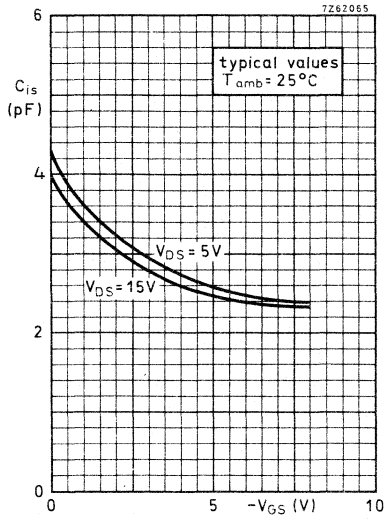




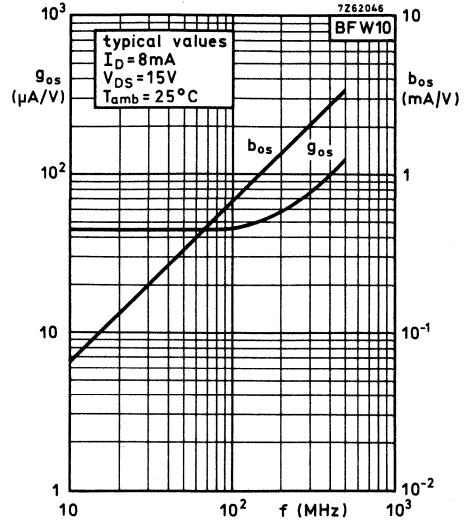
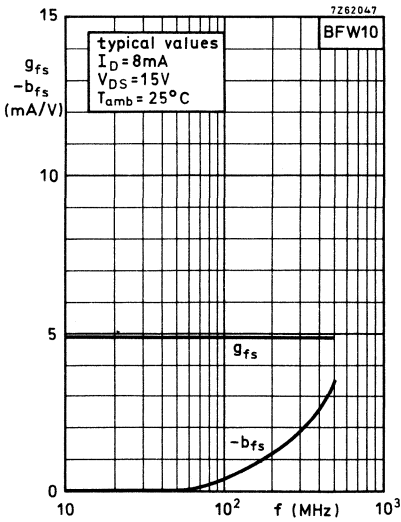
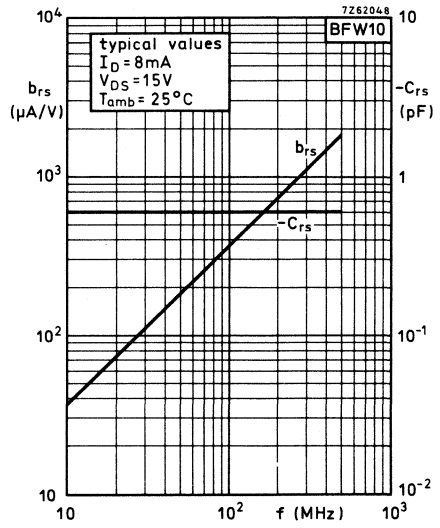
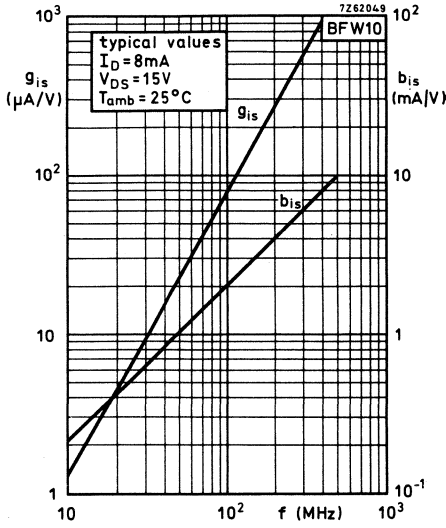


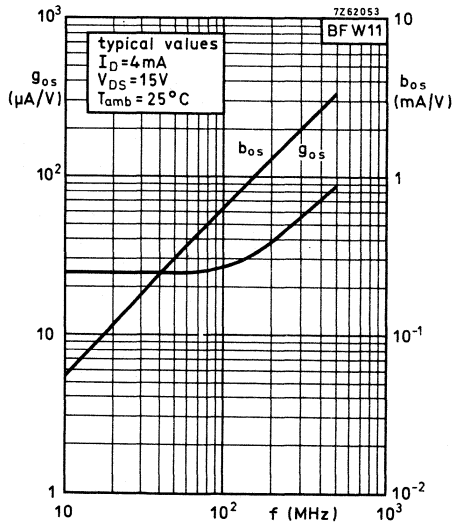
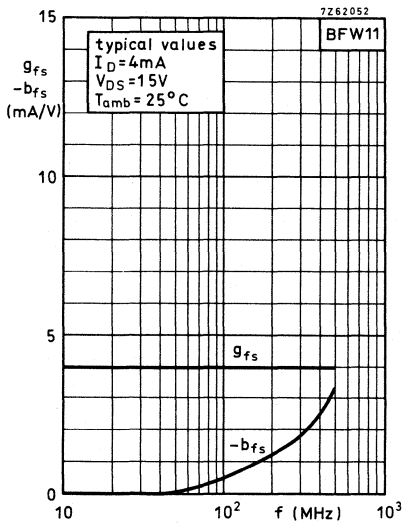
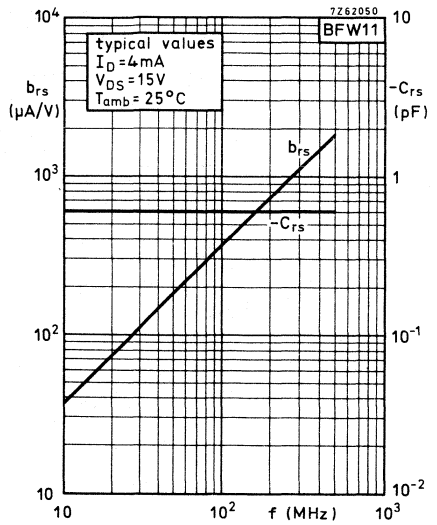
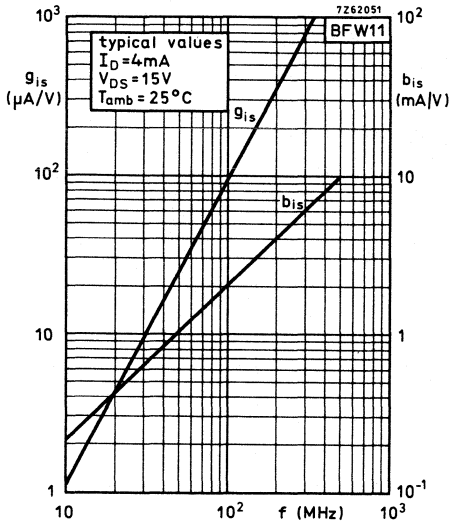
# BFW10 BFW11



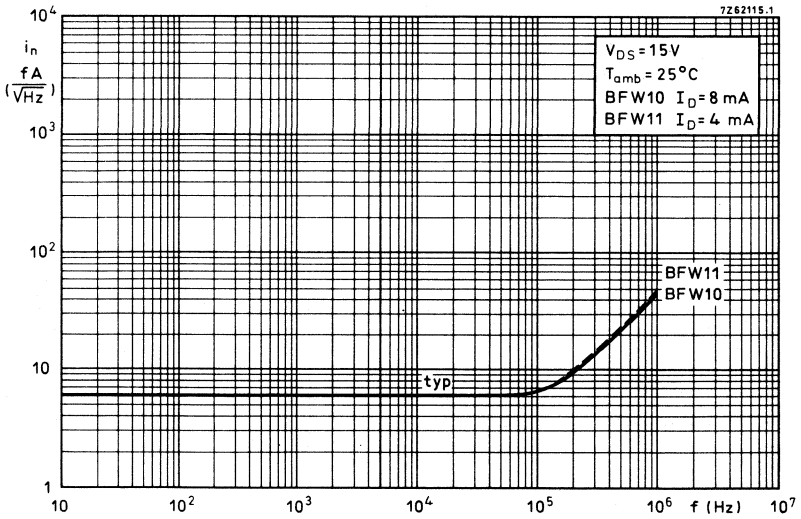
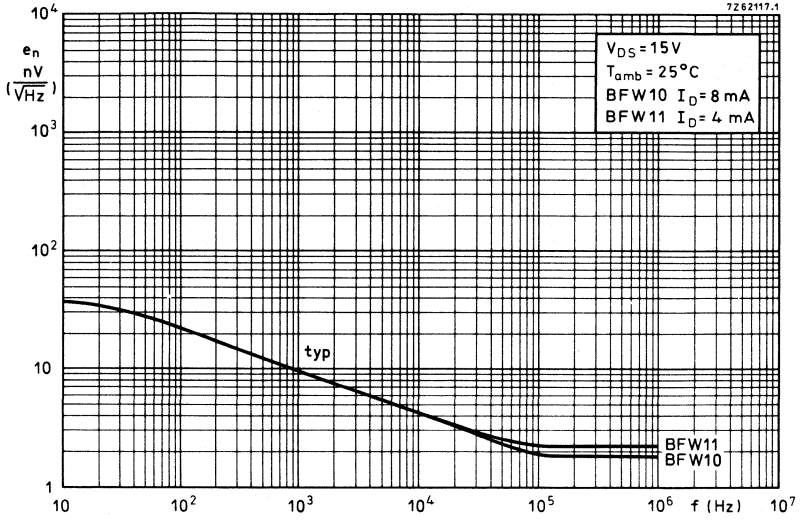


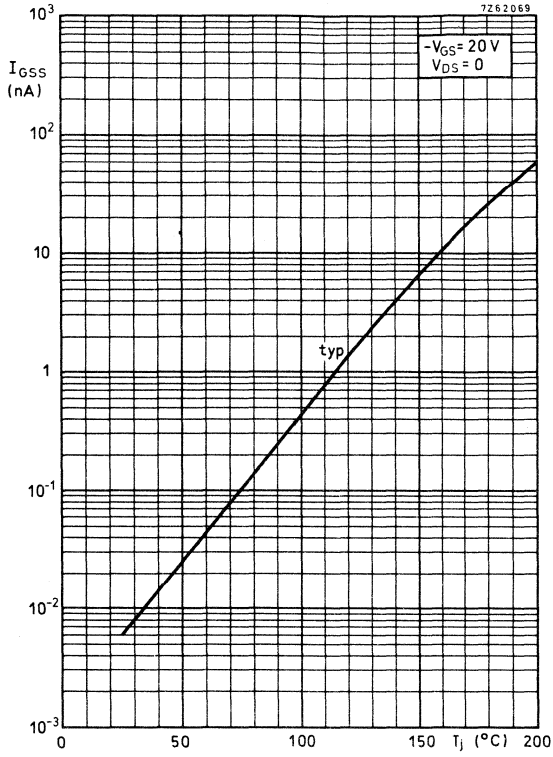
# BFW10 BFW11





**BFW10**  
**BFW11**









## N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

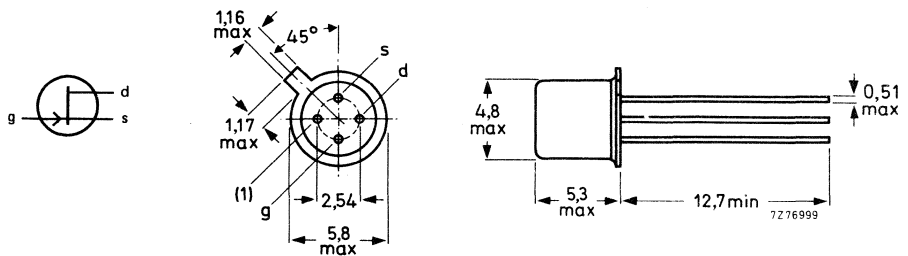
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to $T_{amb} = 110\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	150	mW
			<b>BFW12</b>	<b>BFW13</b>
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	$>$	1	0,2 mA
		$<$	5	1,5 mA
Gate-source cut-off voltage $I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	$<$	2,5	1,2 V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	$C_{rs}$	$<$	0,80	0,80 pF
Transfer admittance (common source) $V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}; f = 1\text{ kHz}$	$ Y_{fs} $	$>$	0,5	0,5 mS
Equivalent noise voltage $V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}$ $B = 0,6\text{ to }100\text{ Hz}$	$V_n$	$<$	0,5	0,5 $\mu\text{V}$

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

**BFW12**  
**BFW13**

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V

Drain current	$I_D$	max.	10 mA
Gate current	$I_G$	max.	5 mA

Total power dissipation up to $T_{amb} = 110\text{ }^\circ\text{C}$	$P_{tot}$	max.	150 mW
---	-----------	------	--------

Storage temperature	$T_{stg}$	-65 to +200	$^\circ\text{C}$
Junction temperature	$T_j$	max.	200 $^\circ\text{C}$

**THERMAL RESISTANCE**

→ From junction to ambient	$R_{th\ j-a}$	=	0.59 K/mW
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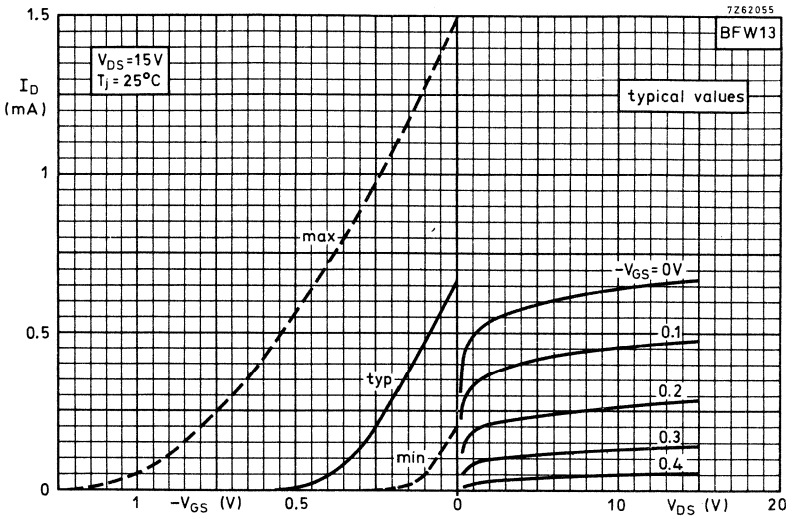
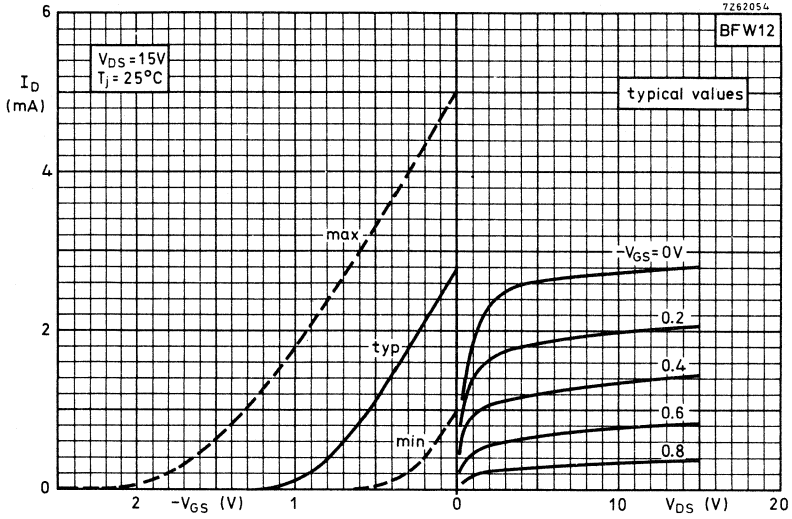
## CHARACTERISTICS

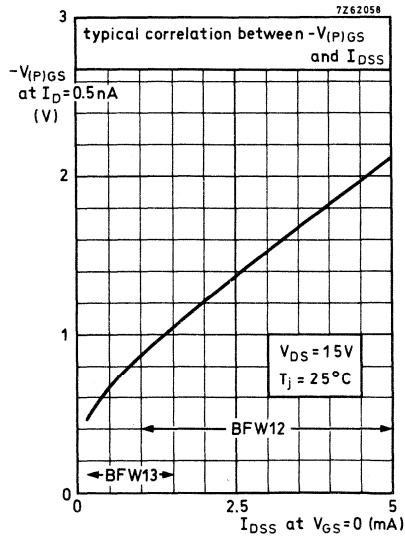
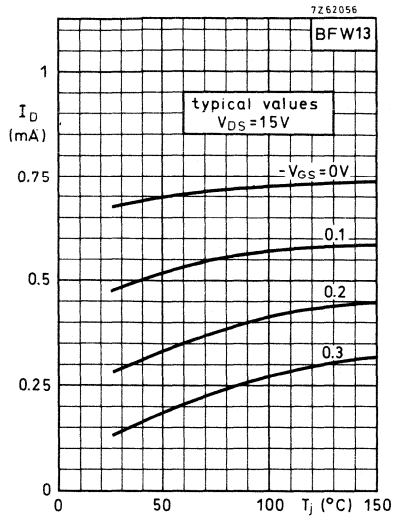
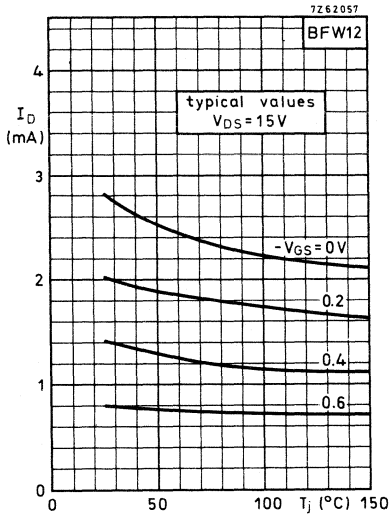
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

		BFW12		BFW13	
Gate cut-off currents					
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS} = 10\text{ V}; V_{DS} = 0; T_j = 150\text{ }^\circ\text{C}$	$-I_{GSS}$	<	0.1	0.1	$\mu\text{A}$
Drain current $I_D$					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
$I_D = 50\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
$I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at $f = 1\text{ kHz}; T_{amb} = 25\text{ }^\circ\text{C}$					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	Transfer admittance	$ y_{fs} $	> 2.0	1.0	mS
	Output admittance	$ y_{os} $	< 30	10	$\mu\text{S}$
$V_{DS} = 15\text{ V}; I_D = 500\text{ }\mu\text{A}$	Transfer admittance	$ y_{fs} $	> 1.5	-	mS
	Output admittance	$ y_{os} $	< 10	-	$\mu\text{S}$
$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}$	Transfer admittance	$ y_{fs} $	> 0.5	0.5	mS
	Output admittance	$ y_{os} $	< 5	5	$\mu\text{S}$
$f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	Input capacitance	$C_{iss}$	< 5	5	pF
	Feedback capacitance	$-C_{rs}$	< 0.80	0.80	pF
Equivalent noise voltage					
$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}; T_{amb} = 25\text{ }^\circ\text{C}$	$V_n$	<	0.5	0.5	$\mu\text{V}$
					B = 0.6 to 100 Hz

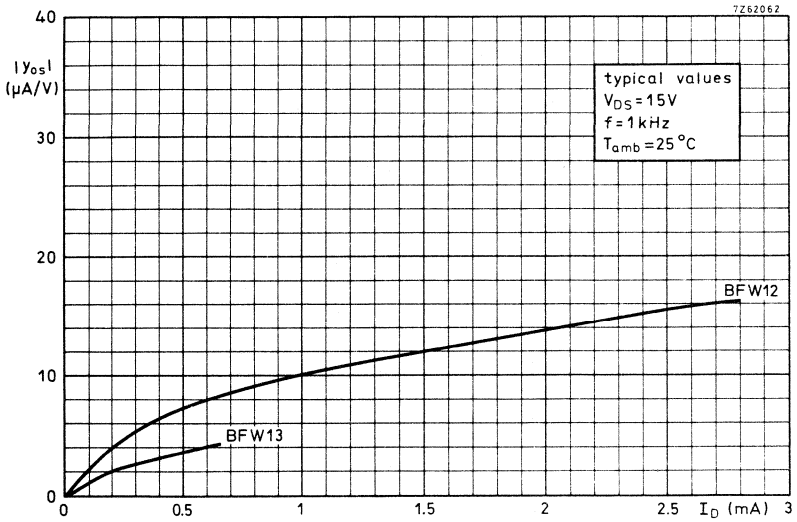
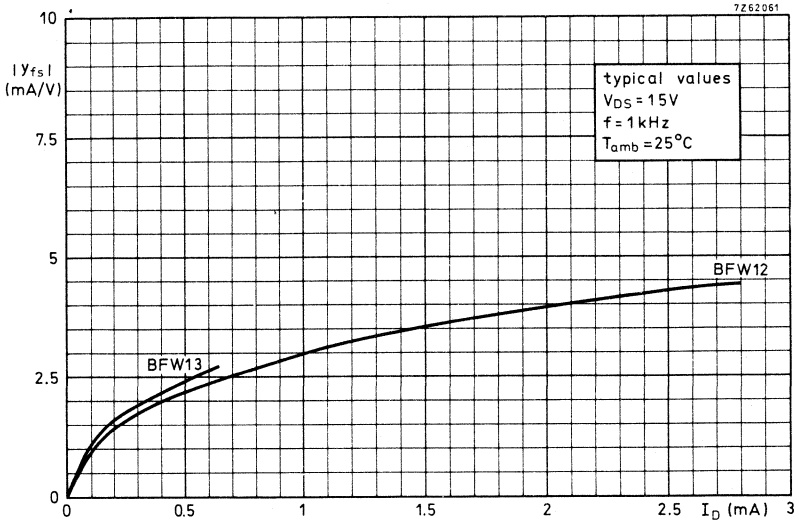
<sup>1)</sup> Measured under pulsed conditions.

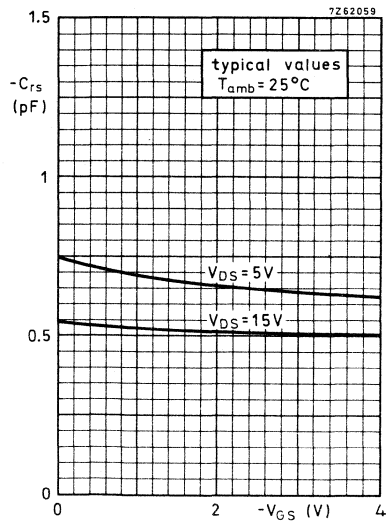
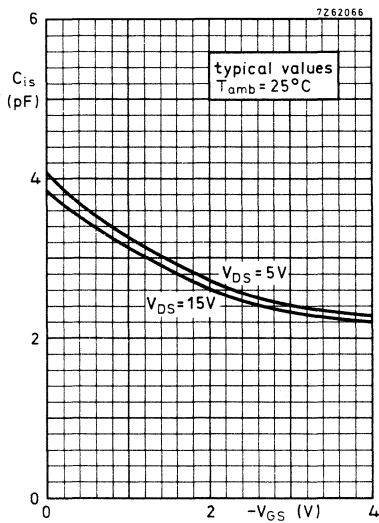
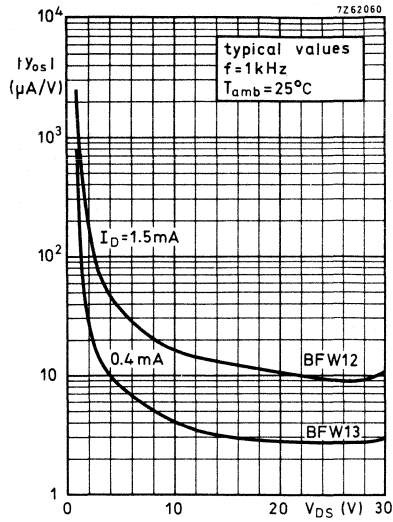
**BFW12**  
**BFW13**



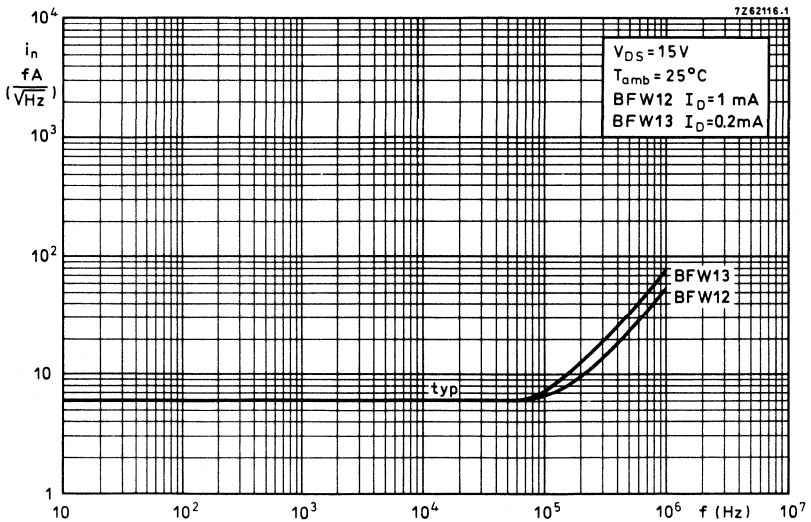
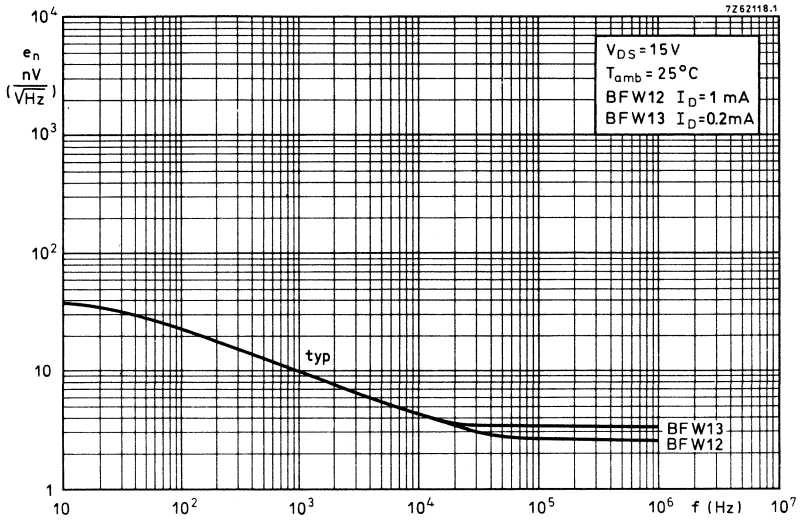


**BFW12**  
**BFW13**

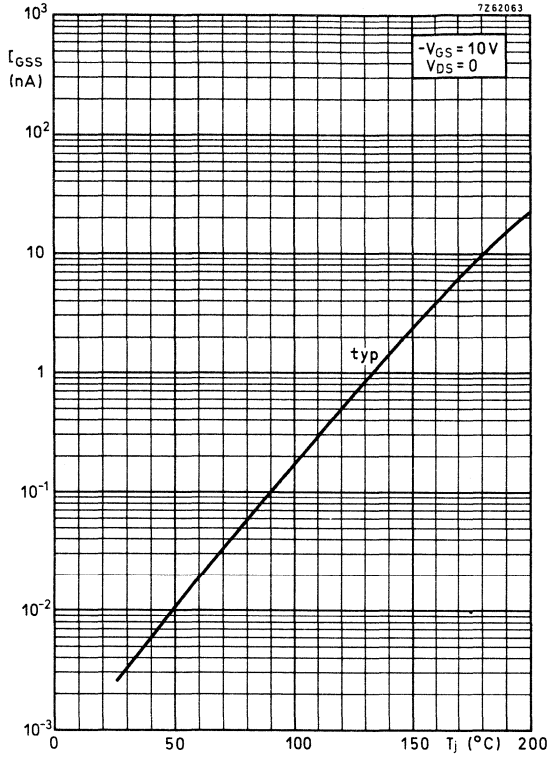




# BFW12 BFW13









## N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

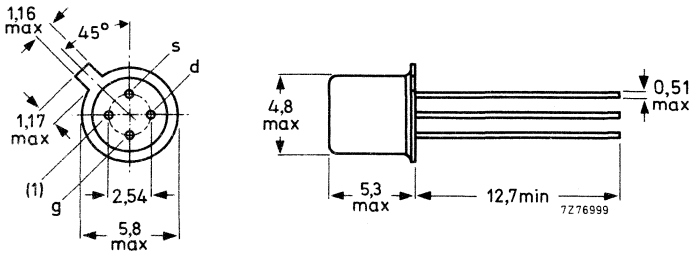
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$		2 to 20 mA
Gate-source cut-off voltage $I_D = 1,0\text{ nA}; V_{DS} = 15\text{ V}$	$-V(P)GS$	<	8 V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	$C_{rs}$	<	2,0 pF
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 10\text{ MHz}$	$ y_{fs} $	>	1,6 mS ←

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	$I_D$	max.	20 mA
Gate current	$I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
Storage temperature	$T_{stg}$		-65 to + 200 $^\circ\text{C}$
Junction temperature	$T_j$	max.	200 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{thj-a}$	=	590 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off currents

$-V_{GS} = 20\text{ V}; V_{DS} = 0$   $-I_{GSS} < 1,0\text{ nA}$

$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 150\text{ }^\circ\text{C}$   $-I_{GSS} < 1,0\text{ }\mu\text{A}$

Drain current\*

$V_{DS} = 15\text{ V}; V_{GS} = 0$   $I_{DSS} \quad 2\text{ to }20\text{ mA}$

Gate-source voltage

$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$   $-V_{GS} \quad 0,5\text{ to }7,5\text{ V}$

Gate-source cut-off voltage

$I_D = 1,0\text{ nA}; V_{DS} = 15\text{ V}$   $-V(P)_{GS} < 8\text{ V}$

y-parameters (common source)

$V_{DS} = 15\text{ V}; V_{GS} = 0$

→ Transfer admittance at  $f = 1\text{ kHz}$   $|Y_{fs}| \quad 2,0\text{ to }6,5\text{ mS}$   
 at  $f = 10\text{ MHz}$   $> 1,6\text{ mS}$

Output admittance at  $f = 1\text{ kHz}$   $|Y_{os}| < 85\text{ }\mu\text{S}$

Input capacitance at  $f = 1\text{ MHz}$   $C_{is} < 6\text{ pF}$

Feedback capacitance at  $f = 1\text{ MHz}$   $C_{rs} < 2,0\text{ pF}$

\* Measured under pulse conditions.

## N-CHANNEL FETS

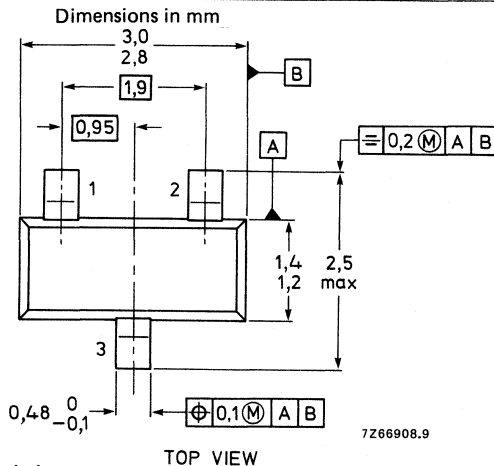
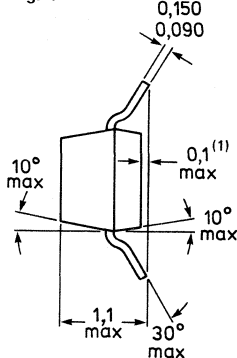
Silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

### QUICK REFERENCE DATA

		BSR56	BSR57	BSR58
Drain-source voltage	$\pm V_{DS}$	max. 40	40	40 V
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}$	$P_{tot}$	max. 250	250	250 mW
Drain current				
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	$> 50$	20	8 mA
		$< -$	100	80 mA
Gate-source cut-off voltage				
$V_{DS} = 15\text{ V}; I_D = 0,5\text{ nA}$	$-V_{(P)GS}$	$> 4$	2	0,8 V
		$< 10$	6	4 V
Drain-source resistance (on) at $f = 1\text{ kHz}$				
$I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	$< 25$	40	60 $\Omega$
Feedback capacitance at $f = 1\text{ MHz}$				
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$C_{rs}$	$< 5$	5	5 pF
Turn-off time				
$V_{DD} = 10\text{ V}; V_{GS} = 0$				
$I_D = 20\text{ mA}; -V_{GSM} = 10\text{ V}$	$t_{off}$	$< 25$	-	- ns
$I_D = 10\text{ mA}; -V_{GSM} = 6\text{ V}$	$t_{off}$	$< -$	50	- ns
$I_D = 5\text{ mA}; -V_{GSM} = 4\text{ V}$	$t_{off}$	$< -$	-	100 ns

### MECHANICAL DATA

Fig. 1 SOT-23.



### Marking code

BSR56 = M4  
BSR57 = M5  
BSR58 = M6



See also *Soldering Recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (See Fig. 4)	$V_{DGO}$	max.	40 V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40 V
Forward gate current	$I_{GF}$	max.	50 mA
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	250 mW
Storage temperature	$T_{stg}$		-55 to + 175 $^{\circ}\text{C}$
Junction temperature	$T_j$	max.	175 $^{\circ}\text{C}$

**THERMAL CHARACTERISTICS\***

$T_j = P (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$

**Thermal resistance**

From junction to tab	$R_{th\ j-t}$	=	60 K/W
From tab to soldering points	$R_{th\ t-s}$	=	280 K/W
From soldering points to ambient**	$R_{th\ s-a}$	=	90 K/W

**CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Gate-source cut-off current

$V_{DS} = 0\text{ V}; -V_{GS} = 20\text{ V}$	$-I_{GSS}$	<	1	nA
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Drain cut-off current

$V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}$	$I_{DSX}$	<	1	nA
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	<b>BSR56</b>	<b>BSR57</b>	<b>BSR58</b>
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Drain current  $\blacktriangle$

$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	50	20	8 mA
		<	-	100	80 mA

Gate-source breakdown voltage

$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V(BR)GSS$	>	40	40	40 V
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Gate-source cut-off voltage

$I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$	$-V(P)GS$	>	4	2	0,8 V
		<	10	6	4 V

Drain-source voltage (on)

$I_D = 20\text{ mA}; V_{GS} = 0$	$V_{DSon}$	<	750	-	- mV
$I_D = 10\text{ mA}; V_{GS} = 0$	$V_{DSon}$	<	-	500	- mV
$I_D = 5\text{ mA}; V_{GS} = 0$	$V_{DSon}$	<	-	-	400 mV

Drain-source resistance (on) at  $f = 1\text{ kHz}$

$I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	<	25	40	60 $\Omega$
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\* See *Thermal characteristics*.

\*\* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

$\blacktriangle$  Measured under pulsed conditions;  $t_p = 100\text{ ms}; \delta \leq 0,1$ .

Switching times\*

$V_{DD} = 10\text{ V}; V_{GS} = 0$   
Conditions  $I_D$  and  $-V_{GSM}$

Delay time  
Rise time  
Turn-off time

		BSR56	BSR57	BSR58
$I_D$	=	20	10	5 mA
$-V_{GSM}$	=	10	6	4 V
Delay time	$t_d$	< 6	6	10 ns
Rise time	$t_r$	< 3	4	10 ns
Turn-off time	$t_{off}$	< 25	50	100 ns

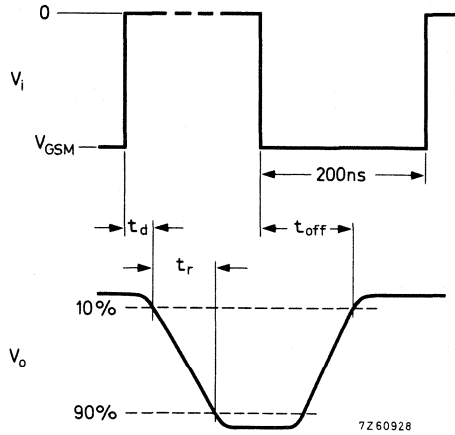


Fig. 2 Switching times waveforms.

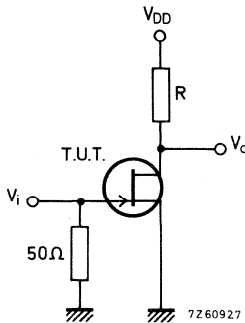


Fig. 3 Test circuit.

BSR56;  $R = 464\ \Omega$   
BSR57;  $R = 953\ \Omega$   
BSR58;  $R = 1910\ \Omega$

Pulse generator

$t_r = t_f \leq 1\text{ ns}$   
 $\delta = 0,02$   
 $Z_0 = 50\ \Omega$

Oscilloscope

$t_r \leq 0,75\text{ ns}$   
 $R_i \geq 1\text{ M}\Omega$   
 $C_i \leq 2,5\text{ pF}$

\* Switching times measured on devices in SOT-18 envelope.

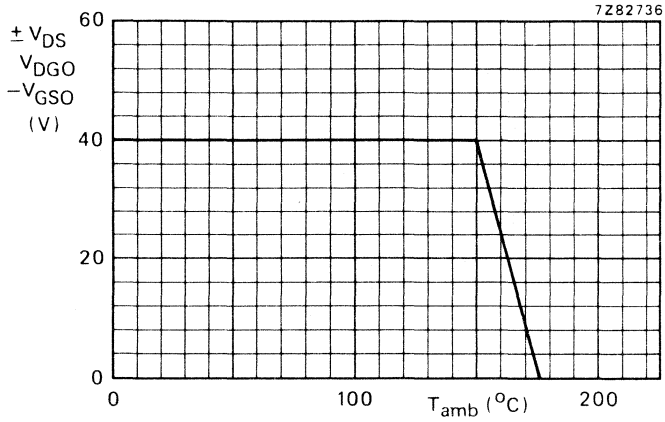


Fig. 4 Voltage derating curve.

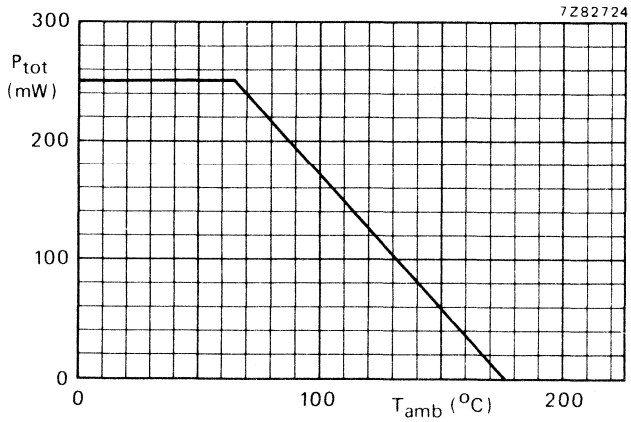


Fig. 5 Power derating curve.



## N-CHANNEL FETS



Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

## QUICK REFERENCE DATA

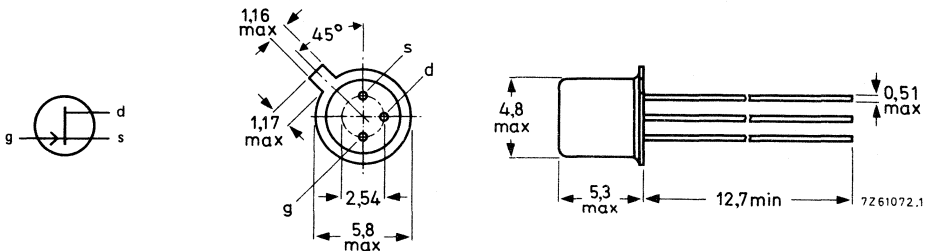
Drain-source voltage	$\pm V_{DS}$	max.	40	V		
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	350	mW		
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	50	20	10	mA
Gate-source cut-off voltage $I_D = 1\text{ nA}; V_{GS} = 15\text{ V}$	$-V_{(P)GS}$	>	3,75	2,0	1,0	V
		<	11	7,0	5,0	V
Drain-source resistance (on) at $f = 1\text{ kHz}$ $I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	<	25	40	60	$\Omega$
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 0; -V_{GS} = 10\text{ V}$	$C_{rs}$	<	5	5	5	pF
Turn-on time	$t_{on}$	<	10	18	30	ns
Turn-off time	$t_{off}$	<	10	16	32	ns

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Accessories: 56246 (distance disc).



Products approved to CECC 50 012-011, available on request.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	40 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40 V
Forward gate current	$I_G$	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	350 mW
Storage temperature	$T_{stg}$		-65 to + 200 $^{\circ}\text{C}$
Operating junction temperature	$T_j$	max.	175 $^{\circ}\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{th\ j-a}$	=	430 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

**Gate cut-off currents**

$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0.25	nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 150\text{ }^\circ\text{C}$	$-I_{GSS}$	<	0.5	$\mu\text{A}$

**Drain cut-off current**

$V_{DS} = 15\text{ V}; -V_{GS} = 12\text{ V}$	$I_{DSX}$	<	0.25	nA
$V_{DS} = 15\text{ V}; -V_{GS} = 12\text{ V}; T_j = 150\text{ }^\circ\text{C}$	$I_{DSX}$	<	0.5	$\mu\text{A}$

**Drain current**

			BSV78	BSV79	BSV80
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	50	20	10 mA

**Gate-source cut-off voltage**

$I_D = 1\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	>	3.75	2.0	1.0 V
		<	11	7.0	5.0 V

**Gate-source voltage**

$I_D = 1.5\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	>	3.5	1.75	0.75 V
		<	10	6.0	4.0 V

**Drain-source voltage (on)**

$I_D = 20\text{ mA}; V_{GS} = 0$	$V_{DSon}$	<	500		mV
$I_D = 10\text{ mA}; V_{GS} = 0$	$V_{DSon}$	<		400	mV
$I_D = 5\text{ mA}; V_{GS} = 0$	$V_{DSon}$	<			325 mV

**Drain-source resistance (on) at  $f = 1\text{ kHz}$**

$I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	<	25	40	60 $\Omega$
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**y parameters at  $f = 1\text{ MHz}$  (common source)**

$-V_{GS} = 10\text{ V}; V_{DS} = 0$					
Input capacitance	$C_{is}$	<	10	10	10 pF
Feedback capacitance	$-C_{rs}$	<	5	5	5 pF

Switching times (see Fig. 2)

Turn-on time when switched from

$-V_{GSMoff} = 11\text{ V}$  to  $I_{Don} = 20\text{ mA}$ ;  $V_{DD} = 10\text{ V}$  (BSV78)

$-V_{GSMoff} = 7\text{ V}$  to  $I_{Don} = 10\text{ mA}$ ;  $V_{DD} = 10\text{ V}$  (BSV79)

$-V_{GSMoff} = 5\text{ V}$  to  $I_{Don} = 5\text{ mA}$ ;  $V_{DD} = 10\text{ V}$  (BSV80)

delay time

rise time

turn-on time

	BSV78	BSV79	BSV80
$t_d$	< 5	10	10 ns
$t_r$	< 5	8	20 ns
$t_{on}$	< 10	18	30 ns

Turn-off time when switched from

$I_{Don} = 20\text{ mA}$  to  $-V_{GSMoff} = 11\text{ V}$ ;  $V_{DD} = 10\text{ V}$  (BSV78)

$I_{Don} = 10\text{ mA}$  to  $-V_{GSMoff} = 7\text{ V}$ ;  $V_{DD} = 10\text{ V}$  (BSV79)

$I_{Don} = 5\text{ mA}$  to  $-V_{GSMoff} = 5\text{ V}$ ;  $V_{DD} = 10\text{ V}$  (BSV80)

fall time

storage time

turn-off time

$t_f$	< 6	11	24 ns
$t_s$	< 4	5	8 ns
$t_{off}$	< 10	16	32 ns

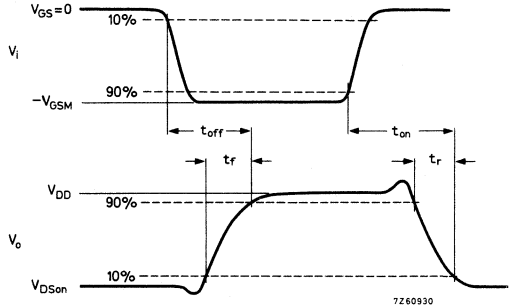
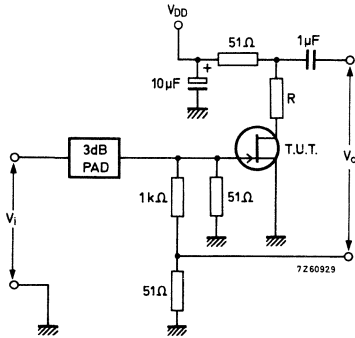


Fig. 2 Switching times test circuit and input and output waveforms.

$$R = \frac{10 - V_{DSon} (V)}{I_{Don} (A)} - 51$$

	BSV78	BSV79	BSV80
R	= 424	909	1885 Ω

Pulse generator:

$R_i = 50\ \Omega$

$t_r < 0,5\text{ ns}$

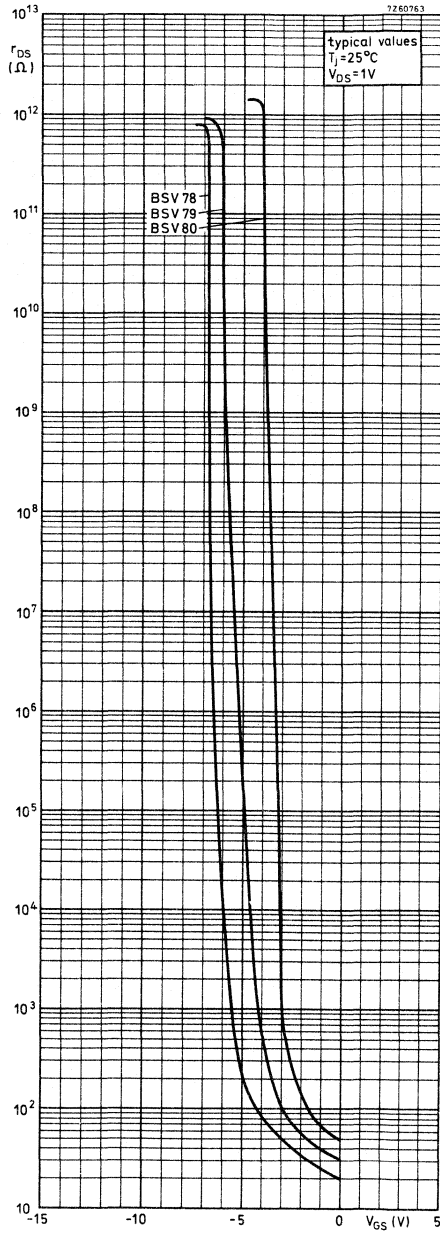
$t_f < 5\text{ ns}$

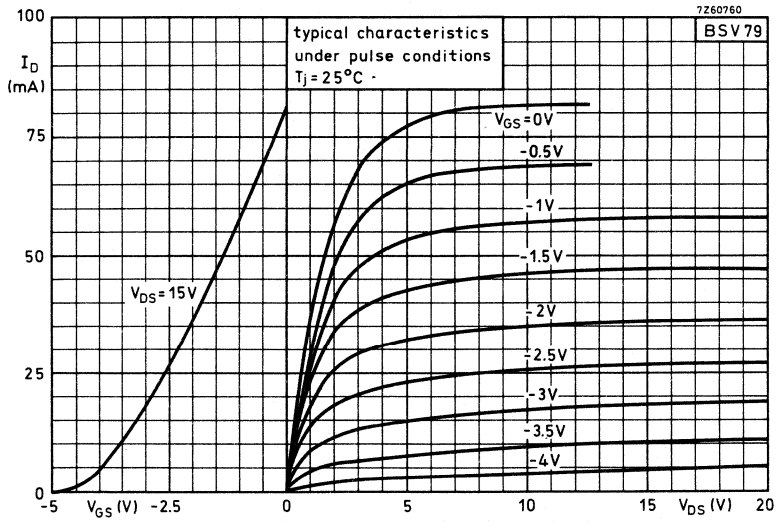
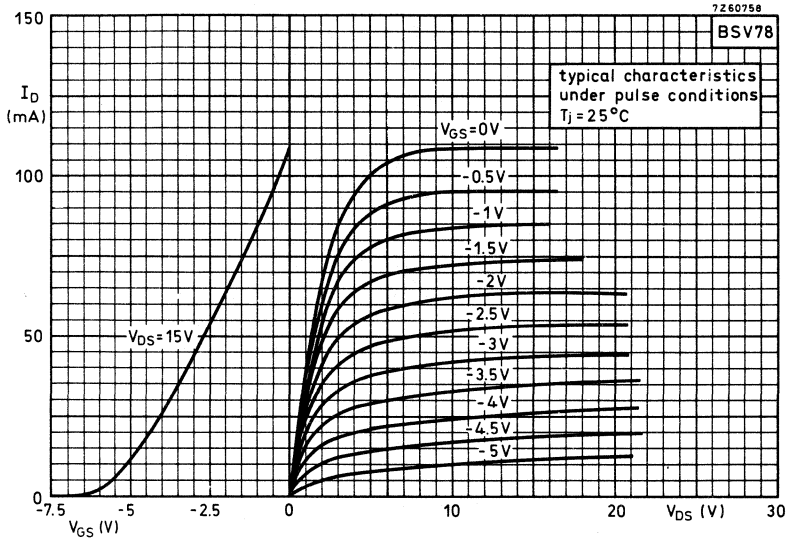
Oscilloscope:

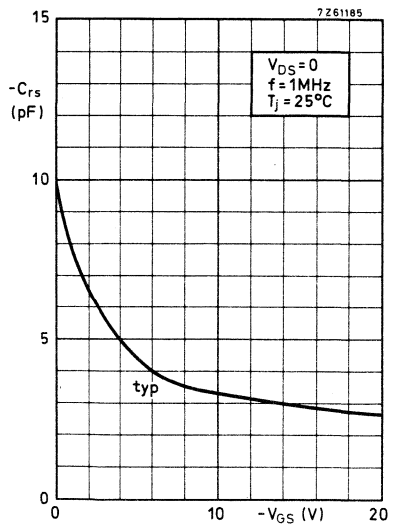
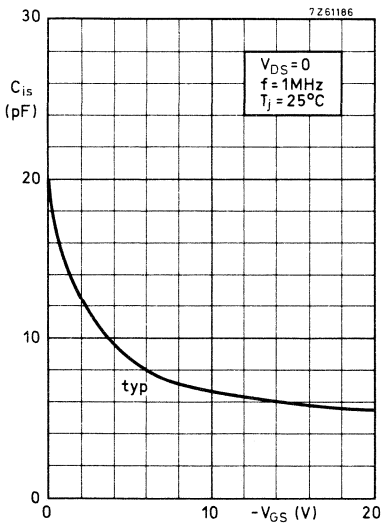
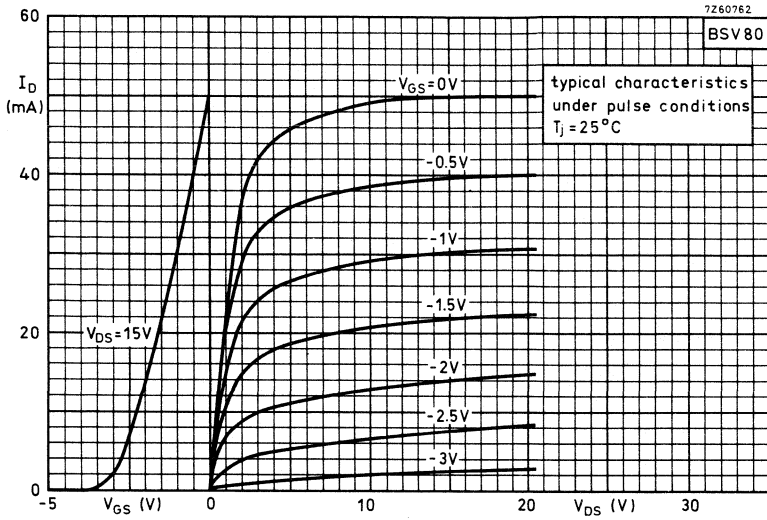
$R_i = 50\ \Omega$

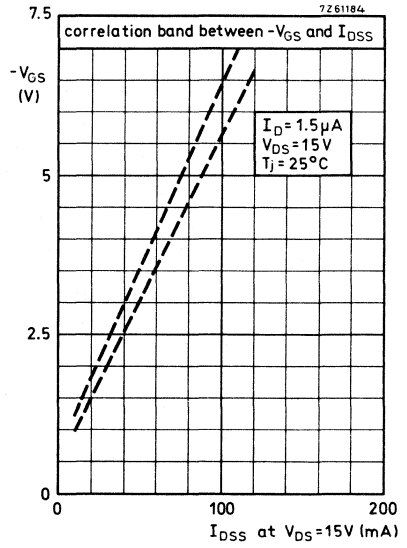
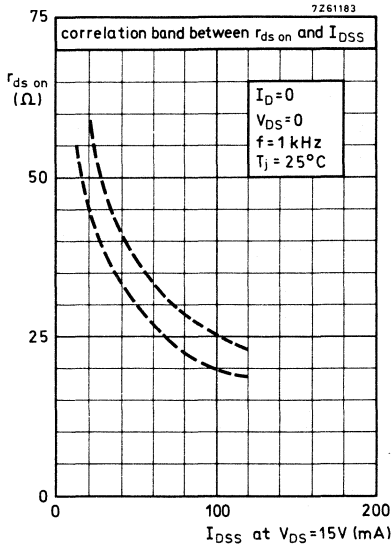
$t_r < 1\text{ ns}$

$t_f < 1\text{ ns}$











## N-CHANNEL FETS

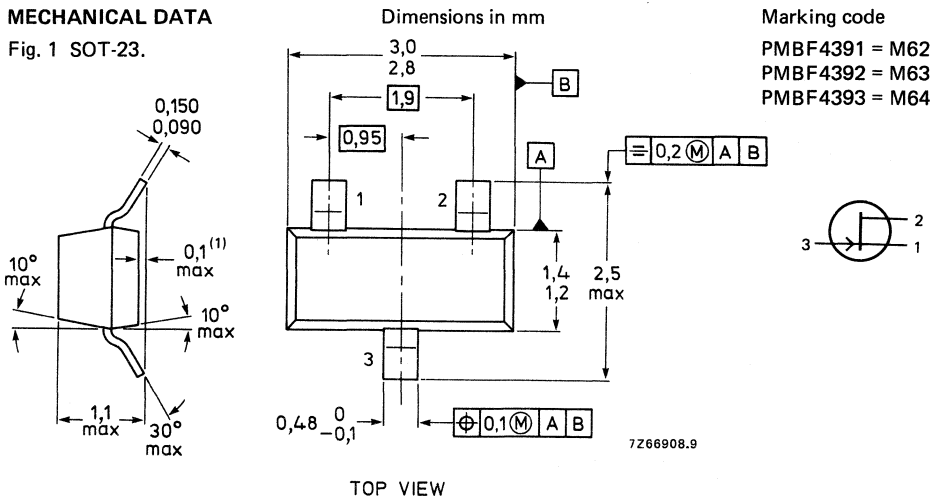
Silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industry.

### QUICK REFERENCE DATA

		PMBF4391	PMBF4392	PMBF4393
Drain-source voltage	$\pm V_{DS}$	max. 40	40	40 V
Drain current $V_{DS} = 20 \text{ V}; V_{GS} = 0$	$I_{DSS}$	> 50	25	5 mA
Gate-source cut-off voltage $V_{DS} = 20 \text{ V}; I_D = 1 \text{ nA}$	$-V_{(P)GS}$	> 4 < 10	2 5	0,5 V 3 V
Drain-source resistance (on) at $f = 1 \text{ kHz}$ $I_D = 1 \text{ mA}; V_{GS} = 0$	$r_{ds\ on}$	< 30	60	100 $\Omega$
Feedback capacitance at $f = 1 \text{ MHz}$ $-V_{GS} = 12 \text{ V}; V_{DS} = 0$	$C_{rs}$	< 3,5	3,5	3,5 pF
Turn-off time $V_{DD} = 10 \text{ V}; V_{GS} = 0$				
$I_D = 12 \text{ mA}; -V_{GSM} = 12 \text{ V}$	$t_{off}$	< 20	—	— ns
$I_D = 6 \text{ mA}; -V_{GSM} = 7 \text{ V}$	$t_{off}$	< —	35	— ns
$I_D = 3 \text{ mA}; -V_{GSM} = 5 \text{ V}$	$t_{off}$	< —	—	50 ns

### MECHANICAL DATA

Fig. 1 SOT-23.



### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (See Fig. 4)	$V_{DGO}$	max.	40 V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40 V
Gate current (d.c.)	$I_G$	max.	50 mA
Total power dissipation up to $T_{amb} = 65^\circ C$	$P_{tot}$	max.	250 mW
Storage temperature	$T_{stg}$		$-65$ to $+175^\circ C$
Junction temperature	$T_j$	max.	175 $^\circ C$

### THERMAL CHARACTERISTICS

$$T_j = P (R_{thj-t} + R_{tht-s} + R_{th s-a}) + T_{amb}$$

Thermal resistance

From junction to tab	$R_{thj-t}$	=	60 K/W
From tab to soldering points	$R_{tht-s}$	=	260 K/W
From soldering points to ambient *	$R_{th s-a}$	=	120 K/W

### CHARACTERISTICS

$T_{amb} = 25^\circ C$  unless otherwise specified

Gate-source voltage

$$I_G = 1 \text{ mA}; V_{DS} = 0 \quad V_{Gson} < 1 \text{ V}$$

Gate-source cut-off current

$$V_{DS} = 0 \text{ V}; -V_{GS} = 20 \text{ V} \quad -I_{GSS} < 1 \text{ nA}$$

$$V_{DS} = 0 \text{ V}; -V_{GS} = 20 \text{ V}; T_{amb} = 150^\circ C \quad -I_{GSS} < 0,2 \mu A$$

		PMBF4391	PMBF4392	PMBF4393
Drain current** $V_{DS} = 20 \text{ V}; V_{GS} = 0$	$I_{DSS} >$	50	25	5 mA
	$I_{DSS} <$	150	75	30 mA
Gate-source breakdown voltage $-I_G = 1 \mu A; V_{DS} = 0$	$-V_{(BR)GSS} >$	40	40	40 V
Gate-source cut-off voltage $I_D = 1 \text{ nA}; V_{DS} = 20 \text{ V}$	$-V_{(P)GS} >$	4	2	0,5 V
	$-V_{(P)GS} <$	10	5	3 V
Drain-source voltage (on) $I_D = 12 \text{ mA}; V_{GS} = 0$ $I_D = 6 \text{ mA}; V_{GS} = 0$ $I_D = 3 \text{ mA}; V_{GS} = 0$	$V_{DSon} <$	0,4	—	— V
	$V_{DSon} <$	—	0,4	— V
	$V_{DSon} <$	—	—	0,4 V
Drain-source resistance (on) $I_D = 0; V_{GS} = 0; f = 1 \text{ kHz}$	$r_{ds on} <$	30	60	100 $\Omega$

\* Mounted on a ceramic substrate of 7 mm x 5 mm x 0,6 mm.

\*\* Measured under pulsed conditions;  $t_p = 100 \mu s; \delta = 0,01$ .

		PMBF4391	PMBF4392	PMBF4393
Drain cut-off current				
$-V_{GS} = 12\text{ V}$	$V_{DS} = 20\text{ V}$	$I_{DSX} < 1$	—	— nA
$-V_{GS} = 7\text{ V}$		$I_{DSX} < -$	1	— nA
$-V_{GS} = 5\text{ V}$		$I_{DSX} < -$	—	1 nA
$-V_{GS} = 12\text{ V}$	$V_{DS} = 20\text{ V}; T_{amb} = 150^\circ\text{C}$	$I_{DSX} < 0,2$	—	— $\mu\text{A}$
$-V_{GS} = 7\text{ V}$		$I_{DSX} < -$	0,2	— $\mu\text{A}$
$-V_{GS} = 5\text{ V}$		$I_{DSX} < -$	—	0,2 $\mu\text{A}$
<b>y-parameters (common source)</b>				
	$V_{DS} = 20\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$			
Input capacitance	$C_{is}$	$< 14$	14	14 pF
Feedback capacitance	$C_{rs}$	$< 3,5$	3,5	3,5 pF
Switching times				
	$V_{DD} = 10\text{ V}; V_{GS} = 0$			
Conditions $I_D$ and $-V_{GSM}$				
	$I_D = 12$	12	6	3 mA
	$-V_{GSM} = 12$	12	7	5 V
Rise time	$t_r$	$< 5$	5	5 ns
Turn on time	$t_{on}$	$< 15$	15	15 ns
Fall time	$t_f$	$< 15$	20	30 ns
Turn off time	$t_{off}$	$< 20$	35	50 ns

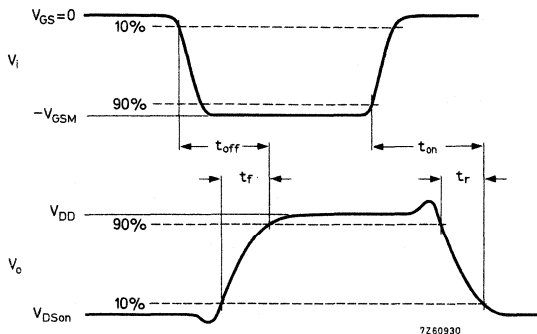
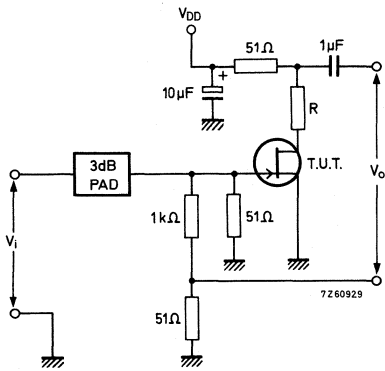


Fig. 2 Switching times waveforms.



$$R = \frac{9,6}{I_D} - 51 \Omega$$

Pulse generator:

- $t_r < 0,5 \text{ ns}$
- $t_f < 0,5 \text{ ns}$
- $t_p = 100 \mu\text{s}$
- $\delta = 0,01$

Oscilloscope:

- $R_i = 50 \Omega$

Fig. 3 Test circuit.

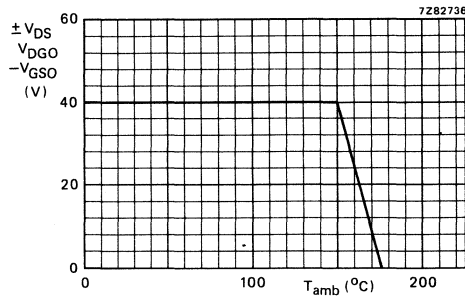


Fig. 4 Voltage derating curve.

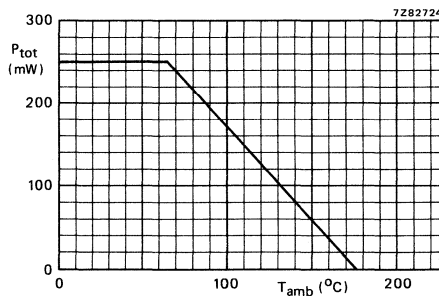


Fig. 5 Power derating curve.

## N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

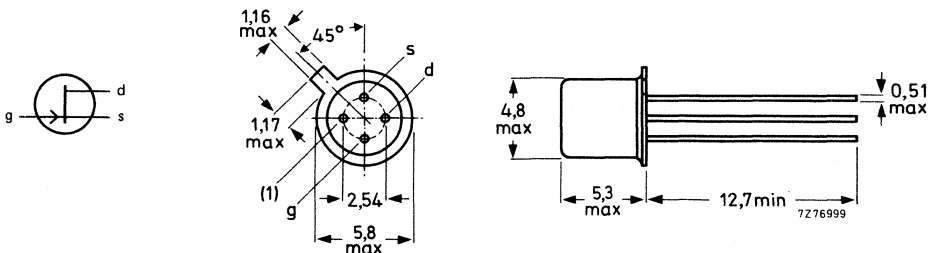
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$		2 to 10 mA
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ y_{fs} $		3,0 to 6,5 mS
$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 100\text{ MHz}$	$ y_{fs} $	>	3,0 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Drain-gate voltage	$V_{DG}$	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Gate current (d.c.)	$I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
Storage temperature	$T_{stg}$		-65 to +200 $^\circ\text{C}$
Junction temperature	$T_j$	max.	200 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{th\ j-a}$	=	590 K/W
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**CHARACTERISTICS** with source connected to case for all measurements

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off current

$-V_{GS} = 30\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,1 nA
$-V_{GS} = 30\text{ V}; V_{DS} = 0; T_{amb} = 150\text{ }^\circ\text{C}$	$-I_{GSS}$	<	0,1 $\mu\text{A}$

Drain current \*

$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$		2 to 10 mA
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Gate-source breakdown voltage

$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	>	50 V
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Gate-source voltage

$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}$	$-V_{GS}$		1 to 4 V
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Gate-source cut-off voltage

$V_{DS} = 15\text{ V}; I_D = 0,5\text{ nA}$	$-V_{(P)GS}$	<	6 V
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**Small-signal common source characteristics**

$V_{DS} = 15\text{ V}; V_{GS} = 0$

→ Transfer admittance \*

$f = 1\text{ kHz}$	$ Y_{fs} $		3,0 to 6,5 mS
$f = 100\text{ MHz}$	$ Y_{fs} $	>	3,0 mS

→ Output admittance at  $f = 1\text{ kHz}$  \*

	$ Y_{os} $	<	20 $\mu\text{S}$
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Input capacitance at  $f = 1\text{ MHz}$

	$C_{is}$	<	6 pF
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Feedback capacitance at  $f = 1\text{ MHz}$

	$C_{rs}$	<	3 pF
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Noise figure

$V_{DS} = 15\text{ V}; V_{GS} = 0; R_G = 1\text{ M}\Omega$			
$f = 10\text{ Hz}; B = 5\text{ Hz}$	F	<	5 dB

Equivalent input noise voltage

$V_{DS} = 15\text{ V}; V_{GS} = 0$			
$f = 10\text{ Hz}; B = 5\text{ Hz}$	$V_n$	<	200 $\text{nV}/\sqrt{\text{Hz}}$

\* Measured under pulse conditions:  $t_p = 100\text{ ms}; \delta \leq 0,1$ .

## N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

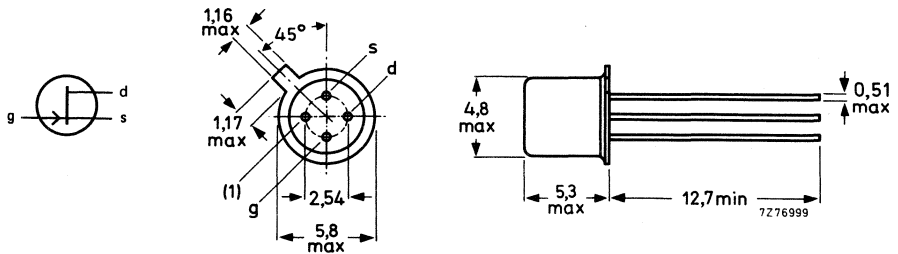
### QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V	
Gate-source voltage	$-V_{GS}$	max.	30 V	
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW	
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$		4 to 20 mA	
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	$C_{rs}$	<	2 pF	
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 200\text{ MHz}$	$ y_{fs} $	>	3,2 mS	←
Noise figure at $f = 100\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0; R_G = 1\text{ k}\Omega$	F	<	2,5 dB	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage	$V_{DG}$	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Gate current (d.c.)	$I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
Storage temperature	$T_{stg}$		-65 to +200 $^\circ\text{C}$
Junction temperature	$T_j$	max.	200 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{th\ j-a}$	=	590 K/W
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**CHARACTERISTICS** with source and shield connected to case for all measurements

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,5 nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 150\text{ }^\circ\text{C}$	$-I_{GSS}$	<	0,5 $\mu\text{A}$

Drain current \*

$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$		4 to 20 mA
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Gate-source breakdown voltage

$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	>	30 V
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Gate-source voltage

$I_D = 400\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$		1,0 to 7,5 V
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Gate-source cut-off voltage

$V_{DS} = 15\text{ V}; I_D = 0,5\text{ nA}$	$-V_{(P)GS}$	<	8 V
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**Small-signal common source characteristics**

$V_{DS} = 15\text{ V}; V_{GS} = 0$

→ Transfer admittance *			
f = 1 kHz	$ Y_{fs} $		3,5 to 6,5 mS
f = 200 MHz	$ Y_{fs} $	>	3,2 mS
→ Output admittance at f = 1 kHz *	$ Y_{os} $	<	35 $\mu\text{S}$
Input capacitance at f = 1 MHz	$C_{is}$	<	6 pF
Feedback capacitance at f = 1 MHz	$C_{rs}$	<	2 pF
Real part of input conductance at f = 200 MHz	$\text{Re}(Y_{is})$	<	0,8 mS
Real part of output conductance at f = 200 MHz	$\text{Re}(Y_{os})$	<	0,2 mS
Noise figure at f = 100 MHz			
$V_{DS} = 15\text{ V}; V_{GS} = 0; R_G = 1\text{ k}\Omega$	F	<	2,5 dB

\* Measured under pulse conditions:  $t_p = 100\text{ ms}; \delta \leq 0,1$ .



## N-CHANNEL SILICON FET

Symmetrical n-channel planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

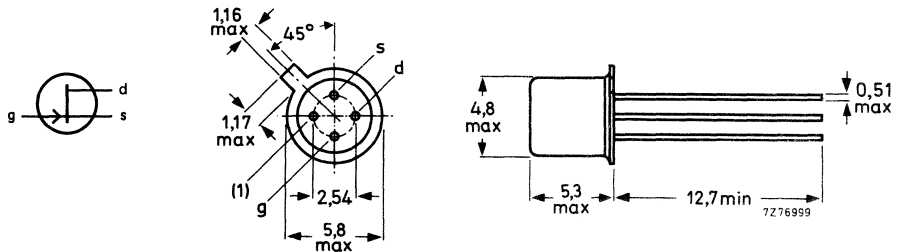
## QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300 mW
Drain current $V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	2 mA
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$		4 to 6 V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 0; V_{GS} = 7\text{ V}$	$C_{rs}$	<	1,5 pF
Drain-source resistance (on) at $f = 1\text{ kHz}$ $V_{GS} = 0; I_D = 0$	$r_{ds\ on}$	<	220 $\Omega$

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	$V_{DGO}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	$I_G$	max.	10	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	300	mW
Storage temperature	$T_{stg}$	-55 to +200		$^{\circ}\text{C}$
Junction temperature	$T_j$	max.	200	$^{\circ}\text{C}$

**THERMAL RESISTANCE**

→ From junction to ambient	$R_{th\ j-a}$	=	0.59	K/mW
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## CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

## Gate cut-off currents

$$-V_{GS} = 20\text{ V}; V_{DS} = 0 \quad -I_{GSS} < 0.1\text{ nA}$$

## Drain current

$$V_{DG} = 20\text{ V}; I_S = 0 \quad I_{DGO} < 0.1\text{ nA}$$

$$V_{DG} = 20\text{ V}; I_S = 0; T_{amb} = 150\text{ }^\circ\text{C} \quad I_{DGO} < 0.2\text{ }\mu\text{A}$$

Drain current <sup>1)</sup>

$$V_{DS} = 20\text{ V}; V_{GS} = 0 \quad I_{DSS} > 2\text{ mA}$$

## Gate-source breakdown voltage

$$-I_G = 1.0\text{ }\mu\text{A}; V_{DS} = 0 \quad -V_{(BR)GS} > 30\text{ V}$$

## Gate-source voltage

$$I_D = 10\text{ nA}; V_{DS} = 10\text{ V} \quad -V_{(P)GS} \quad 4\text{ to }6\text{ V}$$

## Drain-source voltage

$$I_D = 1.0\text{ mA}; V_{GS} = 0 \quad V_{DS} < 0.25\text{ V}$$

## Drain cut-off current

$$V_{DS} = 10\text{ V}; -V_{GS} = 7.0\text{ V} \quad I_D < 1.0\text{ nA}$$

$$V_{DS} = 10\text{ V}; -V_{GS} = 7.0\text{ V}; T_{amb} = 150\text{ }^\circ\text{C} \quad I_D < 2.0\text{ }\mu\text{A}$$

Drain-source resistance (on) at  $f = 1\text{ kHz}$ 

$$V_{GS} = 0; I_D = 0 \quad r_{ds\text{ on}} < 220\text{ }\Omega$$

Input capacitance at  $f = 1\text{ MHz}$ 

$$V_{DS} = 20\text{ V}; V_{GS} = 0 \quad C_{is} < 6\text{ pF}$$

Feedback capacitance at  $f = 1\text{ MHz}$ 

$$V_{DS} = 0; V_{GS} = 7\text{ V} \quad -C_{rs} < 1.5\text{ pF}$$

## CHARACTERISTICS (continued)

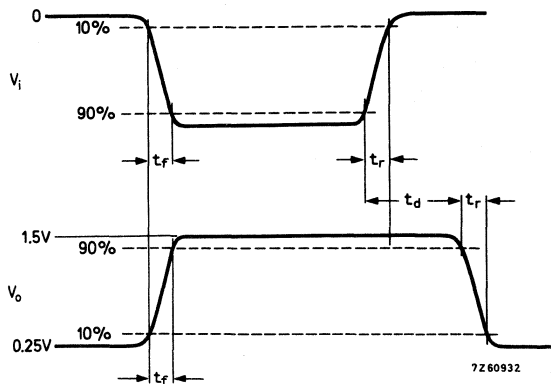
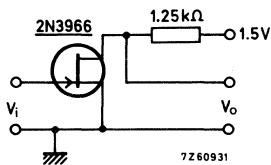
### Switching times

$$V_{DD} = 1.5 \text{ V}; I_{D \text{ on}} = 1.0 \text{ mA}$$

$$V_{GS \text{ on}} = 0; -V_{GS \text{ off}} = 6 \text{ V}$$

delay time	$t_d$	<	20	ns
rise time	$t_r$	<	100	ns
turn off time	$t_{\text{off}}$	<	100	ns

Test circuit:



Pulse generator:

$$t_r < 1.0 \text{ ns}$$

$$t_f < 1.0 \text{ ns}$$

$$t_p = 1.0 \text{ } \mu\text{s}$$

$$\delta < 0.5$$

$$R_S = 50 \text{ } \Omega$$

Oscilloscope:

$$t_r < 10 \text{ ns}$$

$$R_i > 5 \text{ M}\Omega$$

$$C_i < 10 \text{ pF}$$

## N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

### QUICK REFERENCE DATA

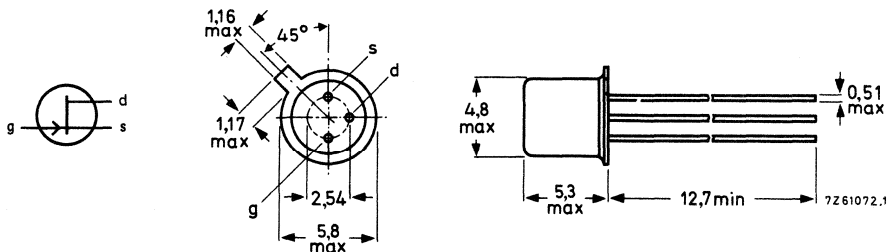
Drain-source voltage	$\pm V_{DS}$	max.	40	V		
Total power dissipation up to $T_{case} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max	1,8	W		
Drain current			<b>2N4091</b>	<b>2N4092</b>	<b>2N4093</b>	
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS}$	$>$	30	15	8	mA
Gate-source cut-off voltage						
$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$	$-V_{(P)GS}$	$>$	5,0	2,0	1,0	V
		$<$	10	7,0	5,0	V
Drain-source resistance (on) at $f = 1\text{ kHz}$						
$I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	$<$	30	50	80	$\Omega$
Feedback capacitance at $f = 1\text{ MHz}$						
$V_{DS} = 0; -V_{GS} = 20\text{ V}$	$C_{rs}$	$<$	5,0			pF
Turn-off time						
$V_{DD} = 3,0\text{ V}; V_{GS} = 0$						
$I_D = 6,6\text{ mA}; -V_{GSM} = 12\text{ V}$	$t_{off}$	$<$		40		ns
$I_D = 4,0\text{ mA}; -V_{GSM} = 8\text{ V}$	$t_{off}$	$<$		60		ns
$I_D = 2,5\text{ mA}; -V_{GSM} = 6\text{ V}$	$t_{off}$	$<$		80		ns
			<b>2N4091</b>	<b>2N4092</b>	<b>2N4093</b>	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Accessories: 56246 (distance disc).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	40 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40 V

Current

Forward gate current (d. c.)	$I_G$	max.	10 mA
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Total power dissipation up to $T_{case} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	1.8 W
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Storage temperature	$T_{stg}$	-55 to +200	$^{\circ}\text{C}$
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Junction temperature	$T_j$	max.	200 $^{\circ}\text{C}$
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**THERMAL RESISTANCE**

→ From junction to case in free air	$R_{th\ j-c}$	=	0.1 K/mW
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**CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Drain currents**

$V_{DG} = 20\text{ V}; I_S = 0$   $I_{DGO} < 0.2\text{ nA}$

$V_{DG} = 20\text{ V}; I_S = 0; T_{amb} = 150\text{ }^{\circ}\text{C}$   $I_{DGO} < 0.4\text{ }\mu\text{A}$

**Source current**

$V_{SG} = 20\text{ V}; I_D = 0$   $I_{SGO} < 0.2\text{ nA}$

**Drain cut-off current**

		2N4091	2N4092	2N4093
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}$	$I_{DSX} <$	0.2	-	- nA
$V_{DS} = 20\text{ V}; -V_{GS} = 8\text{ V}$	$I_{DSX} <$	-	0.2	- nA
$V_{DS} = 20\text{ V}; -V_{GS} = 6\text{ V}$	$I_{DSX} <$	-	-	0.2 nA
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	0.4	-	- $\mu\text{A}$
$V_{DS} = 20\text{ V}; -V_{GS} = 8\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	-	0.4	- $\mu\text{A}$
$V_{DS} = 20\text{ V}; -V_{GS} = 6\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	-	-	0.4 $\mu\text{A}$

**Gate-source breakdown voltage**

$-I_G = 1.0\text{ }\mu\text{A}; V_{DS} = 0$   $-V_{(BR)GSS} > 40\text{ V}$

**Drain current <sup>1)</sup>**

$V_{DS} = 20\text{ V}; V_{GS} = 0$   $I_{DSS} > 30\text{ mA}$

**Gate-source cut-off voltage**

$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$   $-V_{(P)GS} > 5.0\text{ V}$

**Drain-source voltages (on)**

$I_D = 6.6\text{ mA}; V_{GS} = 0$   $V_{DSon} < 0.2\text{ V}$

$I_D = 4.0\text{ mA}; V_{GS} = 0$   $V_{DSon} < 0.2\text{ V}$

$I_D = 2.5\text{ mA}; V_{GS} = 0$   $V_{DSon} < 0.2\text{ V}$

**Drain-source resistance (on)**

$I_D = 1.0\text{ mA}; V_{GS} = 0$   $r_{DSon} < 30\text{ }\Omega$

**Drain-source resistance (on) at  $f = 1\text{ kHz}$**

$I_D = 0; V_{GS} = 0$   $r_{ds\text{ on}} < 30\text{ }\Omega$

<sup>1)</sup> Measured under pulsed conditions:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.03$

## CHARACTERISTICS (continued)

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

y-parameters at  $f = 1\text{ MHz}$  (common source)

Input capacitance

$$V_{DS} = 20\text{ V} ; V_{GS} = 0$$

$$C_{is} < 16\text{ pF}$$

Feedback capacitance

$$V_{DS} = 0 ; -V_{GS} = 20\text{ V}$$

$$C_{rs} < 5\text{ pF}$$

Switching times

$$V_{DD} = 3.0\text{ V} ; V_{GS} = 0$$

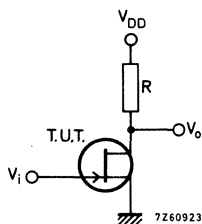
Delay time

Rise time

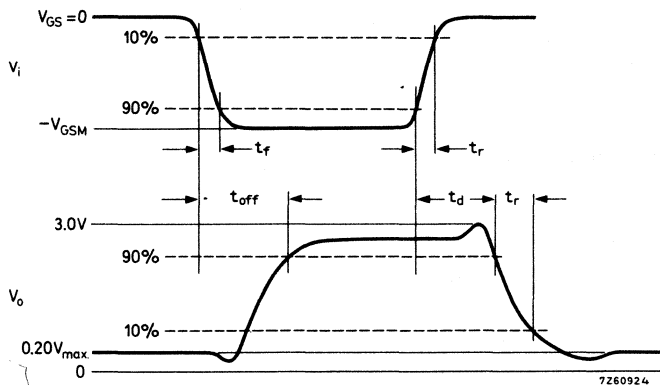
Turn-off time

	2N4091	2N4092	2N4093	
$I_D =$	6,6	4,0	2,5	mA
$-V_{GSM} =$	12	8	6	V
$t_d <$	15	15	20	ns
$t_r <$	10	20	40	ns
$t_{off} <$	40	60	80	ns

Test circuit:



$$R = \frac{2,8}{I_D}$$



Pulse generator:

$t_r <$	1	ns
$t_f <$	1	ns
$t_p =$	1,0	$\mu\text{s}$
$\delta =$	0,1	
$R_S =$	50	$\Omega$

Oscilloscope:

$t_r <$	0,4	ns
$R_i >$	9,8	$M\Omega$
$C_i <$	1,7	pF



## N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

## QUICK REFERENCE DATA

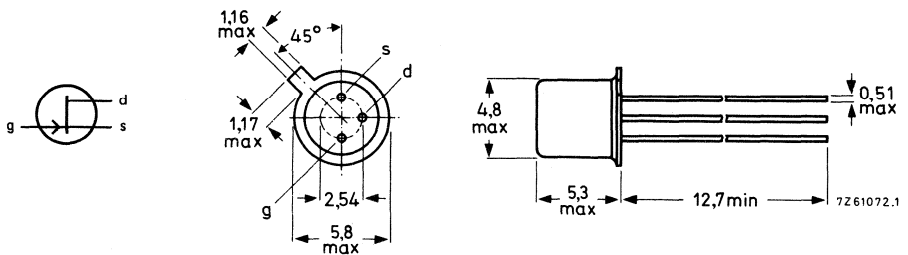
Drain-source voltage	$\pm V_{DS}$	max.	40	V	
Total power dissipation up to $T_{case} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	1,8	W	
Drain current			<b>2N4391</b>	<b>2N4392</b>	<b>2N4393</b>
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS}$	>	50	25	5 mA
Gate-source cut-off voltage					
$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$	$-V_{(P)GS}$	>	4,0	2,0	0,5 V
		<	10	5,0	3,0 V
Drain-source resistance (on) at $f = 1\text{ kHz}$					
$I_D = 1\text{ mA}; V_{GS} = 0$	$r_{ds\ on}$	<	30	60	100 $\Omega$
Feedback capacitance at $f = 1\text{ MHz}$					
$V_{DS} = 0; -V_{GS} = 12\text{ V}$	$C_{rs}$	<	3,5	3,5	3,5 pF
$V_{DS} = 0; -V_{GS} = 7\text{ V}$					
$V_{DS} = 0; -V_{GS} = 5\text{ V}$					
Turn-off time					
$V_{DD} = 10\text{ V}; V_{GS} = 0$	$t_{off}$	<	20	—	— ns
$I_D = 12\text{ mA}; -V_{GSM} = 12\text{ V}$	$t_{off}$	<	—	35	— ns
$I_D = 6,0\text{ mA}; -V_{GSM} = 7\text{ V}$	$t_{off}$	<	—	—	50 ns
$I_D = 3,0\text{ mA}; -V_{GSM} = 5\text{ V}$	$t_{off}$	<	—	—	— ns

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Accessories: 56246 (distance disc).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	$V_{DGO}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (d. c.)	$I_G$	max.	50	mA
Total power dissipation up to $T_{Case} = 25^\circ C$	$P_{tot}$	max.	1.8	W
Storage temperature	$T_{stg}$	-65 to	200	$^\circ C$
Junction temperature	$T_j$	max.	200	$^\circ C$
→ From junction to case in free air	$R_{th\ j-c}$	=	0.1	K/mW

**CHARACTERISTICS**

$T_{amb} = 25^\circ C$  unless otherwise specified

Gate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS} <$	0.1	nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 150^\circ C$	$-I_{GSS} <$	0.2	$\mu A$

Drain cut-off current

		2N4391	2N4392	2N4393	
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}$	$I_{DSX} <$	0.1	-	-	nA
$V_{DS} = 20\text{ V}; -V_{GS} = 7\text{ V}$	$I_{DSX} <$	-	0.1	-	nA
$V_{DS} = 20\text{ V}; -V_{GS} = 5\text{ V}$	$I_{DSX} <$	-	-	0.1	nA
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}; T_{amb} = 150^\circ C$	$I_{DSX} <$	0.2	-	-	$\mu A$
$V_{DS} = 20\text{ V}; -V_{GS} = 7\text{ V}; T_{amb} = 150^\circ C$	$I_{DSX} <$	-	0.2	-	$\mu A$
$V_{DS} = 20\text{ V}; -V_{GS} = 5\text{ V}; T_{amb} = 150^\circ C$	$I_{DSX} <$	-	-	0.2	$\mu A$

## CHARACTERISTICS (continued)

 $T_{amb} = 25^{\circ}\text{C}$  unless otherwise specified

		2N4391	2N4392	2N4393
Drain currents <sup>1)</sup>				
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS} >$	50	-	- mA
	$I_{DSS} <$	150	-	- mA
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS} >$	-	25	- mA
	$I_{DSS} <$	-	75	- mA
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS} >$	-	-	5 mA
	$I_{DSS} <$	-	-	30 mA
Gate-source breakdown voltage				
$-I_G = 1\ \mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS} >$	40	40	40 V
Gate-source voltage				
$I_G = 1\ \text{mA}; V_{DS} = 0$	$V_{GSon} <$	1.0	1.0	1.0 V
Gate-source cut-off voltage				
$I_D = 1\ \text{nA}; V_{DS} = 20\text{ V}$	$-V_{(P)GS} >$	4.0	2.0	0.5 V
	$-V_{(P)GS} <$	10	5.0	3.0 V
Drain-source voltage (on)				
$I_D = 12\ \text{mA}; V_{GS} = 0$	$V_{DSon} <$	0.4	-	- V
$I_D = 6.0\ \text{mA}; V_{GS} = 0$	$V_{DSon} <$	-	0.4	- V
$I_D = 3.0\ \text{mA}; V_{GS} = 0$	$V_{DSon} <$	-	-	0.4 V
Drain-source resistance (on)				
$I_D = 1\ \text{mA}; V_{GS} = 0$	$r_{DSon} <$	30	60	100 $\Omega$
Drain-source resistance (on) at $f = 1\ \text{kHz}$				
$I_D = 0; V_{GS} = 0$	$r_{dson} <$	30	60	100 $\Omega$
y parameters at $f = 1\ \text{MHz}$ (common source)				
Input capacitance				
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$C_{is} <$	14	14	14 pF
Feedback capacitance				
$-V_{GS} = 12\text{ V}; V_{DS} = 0$	$-C_{rs} <$	3.5	-	- pF
$-V_{GS} = 7\text{ V}; V_{DS} = 0$	$-C_{rs} <$	-	3.5	- pF
$-V_{GS} = 5\text{ V}; V_{DS} = 0$	$-C_{rs} <$	-	-	3.5 pF

<sup>1)</sup> measured under pulsed conditions:  $t_p = 100\ \mu\text{s}; \delta = 0.01$

## CHARACTERISTICS (continued)

$T_{amb} = 25^{\circ}\text{C}$  unless otherwise specified

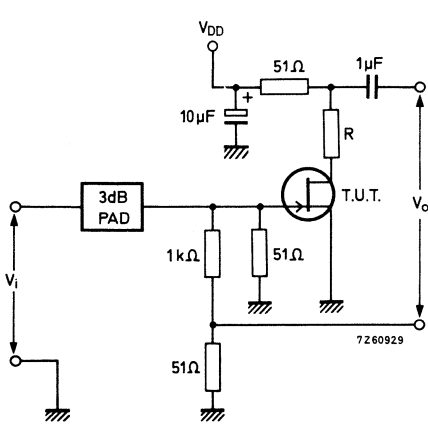
### Switching times

$$V_{DD} = 10\text{ V}; V_{GS} = 0$$

Rise time  
Turn on time  
Fall time  
Turn off time

	2N4391	2N4392	2N4393	
$I_D$	= 12	6.0	3.0	mA
$-V_{GSM}$	= 12	7	5	V
$t_r$	< 5	5	5	ns
$t_{on}$	< 15	15	15	ns
$t_f$	< 15	20	30	ns
$t_{off}$	< 20	35	50	ns

Test circuit:



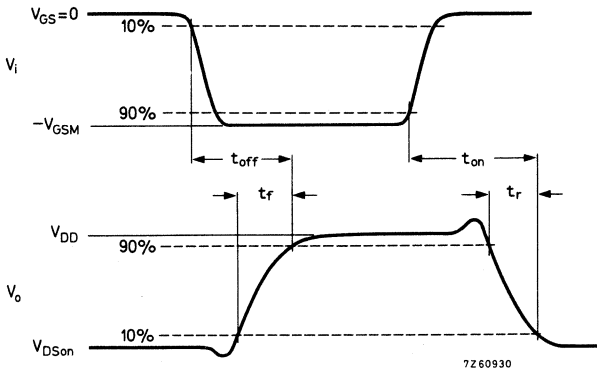
$$R = \frac{9.6}{I_D} - 51\Omega$$

Pulse generator:

$t_r$	< 0.5 ns
$t_f$	< 0.5 ns
$t_p$	= 100 µs
$\delta$	= 0.01

Oscilloscope:

$$R_i = 50\Omega$$



## N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

### QUICK REFERENCE DATA

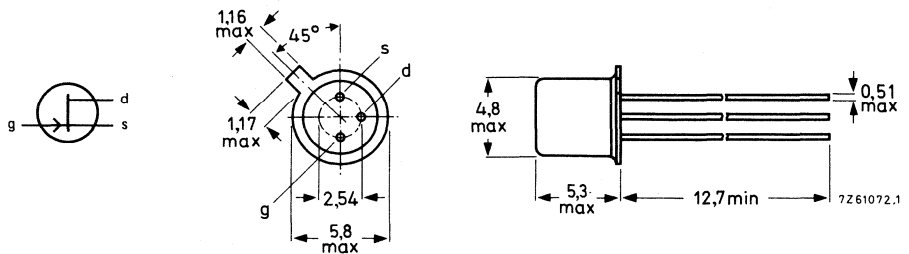
Drain-source voltage	<b>2N4856 to 2N4858</b>	$\pm V_{DS}$	max.	40	V	
	<b>2N4859 to 2N4861</b>	$\pm V_{DS}$	max.	30	V	
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$		$P_{tot}$	max.	360	mW	
Drain current				<b>2N4856</b>	<b>2N4857</b>	<b>2N4858</b>
$V_{DS} = 15\text{ V}; V_{GS} = 0$		$I_{DSS}$	>	50	20	8
Gate-source cut-off voltage						
$I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$		$-V_{(P)GS}$	>	4	2	0,8
			<	10	6	4
Drain-source resistance (on) at $f = 1\text{ kHz}$						
$I_D = 0; V_{GS} = 0$		$r_{ds\ on}$	<	25	40	60
Feedback capacitance at $f = 1\text{ MHz}$						
$V_{DS} = 0; -V_{GS} = 10\text{ V}$		$C_{rs}$	<	8		pF
Turn-off time						
$V_{DD} = 10\text{ V}; V_{GS} = 0$						
$I_D = 20\text{ mA}; -V_{GSM} = 10\text{ V}$	<b>2N4856; 2N4859</b>	$t_{off}$	<	25		ns
$I_D = 10\text{ mA}; -V_{GSM} = 6\text{ V}$	<b>2N4857; 2N4860</b>	$t_{off}$	<	50		ns
$I_D = 5\text{ mA}; -V_{GSM} = 4\text{ V}$	<b>2N4858; 2N4861</b>	$t_{off}$	<	100		ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18

Gate connected to case



Accessories: 56246 (distance disc).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

		2N4856	2N4859	
		2N4857	2N4860	
		2N4858	2N4861	
Drain-source voltage	$\pm V_{DS}$	max. 40	30	V
Drain-gate voltage (open source)	$V_{DGO}$	max. 40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max. 40	30	V
Gate current (d.c.)	$I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 25^\circ C$	$P_{tot}$	max.	360	mW
Storage temperature	$T_{stg}$	-65 to	+200	$^\circ C$
Junction temperature	$T_j$	max.	200	$^\circ C$
<b>THERMAL RESISTANCE</b>				
→ From junction to ambient in free air	$R_{th\ j-a}$	=	0.49	K/mW

**CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

		2N4856	2N4857	2N4858	2N4859	2N4860	2N4861
<b>Gate cut-off currents</b>							
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS} <$	0.25	-	-	-	-	nA
$-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS} <$	-	0.25	-	-	-	nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 150\text{ }^{\circ}\text{C}$	$-I_{GSS} <$	0.5	-	-	-	-	$\mu\text{A}$
$-V_{GS} = 15\text{ V}; V_{DS} = 0; T_{amb} = 150\text{ }^{\circ}\text{C}$	$-I_{GSS} <$	-	0.5	-	-	-	$\mu\text{A}$
<b>Drain cut-off current</b>							
$V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}$	$I_{DSX} <$	0.25	0.25	-	-	-	nA
$V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	0.5	0.5	-	-	-	$\mu\text{A}$
<b>Drain current <sup>1)</sup></b>							
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS} >$	50	20	8	8	8	mA
	$I_{DSS} <$	-	100	80	80	80	mA
<b>Gate-source breakdown voltage</b>							
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	40	30	-	-	-	V
<b>Gate-source cut-off voltage</b>							
$I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS} >$	4	2	0.8	0.8	0.8	V
	$-V_{(P)GS} <$	10	6	4	4	4	V
<b>Drain-source voltage (on)</b>							
$I_D = 20\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	0.75	-	-	-	-	V
$I_D = 10\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	-	0.50	-	-	-	V
$I_D = 5\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	-	-	0.50	-	-	V
<b>Drain-source resistance (on) at <math>f = 1\text{ kHz}</math></b>							
$I_D = 0; V_{GS} = 0$	$r_{dson} <$	25	40	60	60	60	$\Omega$

<sup>1)</sup> measured under pulsed conditions:  $t_p = 100\text{ ms}; \delta \leq 0.1$

**y-parameters (common source)**

$V_{DS} = 0; -V_{GS} = 10 \text{ V}; f = 1 \text{ MHz}$

Input capacitance

Feedback capacitance

$C_{is}$	<	18	pF
$C_{rs}$	<	8	pF

**Switching times (see Figs 2 and 3)**

$V_{DD} = 10 \text{ V}; V_{GS} = 0$

Drain current

Gate-source voltage (peak value)

Delay time

Rise time

Turn-off time

	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
$I_D$	= 20	10	5	mA
$-V_{GSM}$	= 10	6	4	V
$t_d$	< 6	6	10	ns
$t_r$	< 3	4	10	ns
$t_{off}$	< 25	50	100	ns

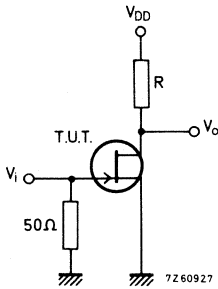


Fig. 2 Switching times test circuit.

2N4856 2N4859	2N4857 2N4860	2N4858 2N4861
R = 464	953	1910

$\Omega$

**Pulse generator:**

$t_r \leq 1 \text{ ns}$

$t_f \leq 1 \text{ ns}$

$\delta = 0,02$

$Z_o = 50 \Omega$

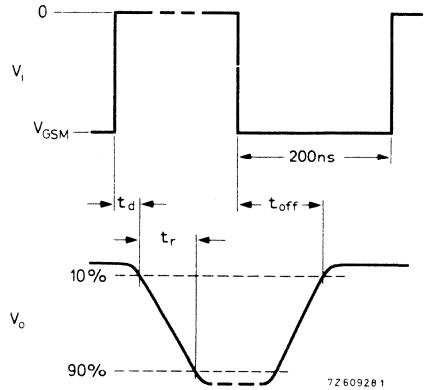


Fig. 3 Input and output waveforms.

**Oscilloscope:**

$t_r \leq 0,75 \text{ ns}$

$R_i \geq 1 \text{ M}\Omega$

$C_i \leq 2,5 \text{ pF}$



DEVICE DATA  
MOS-FETS



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

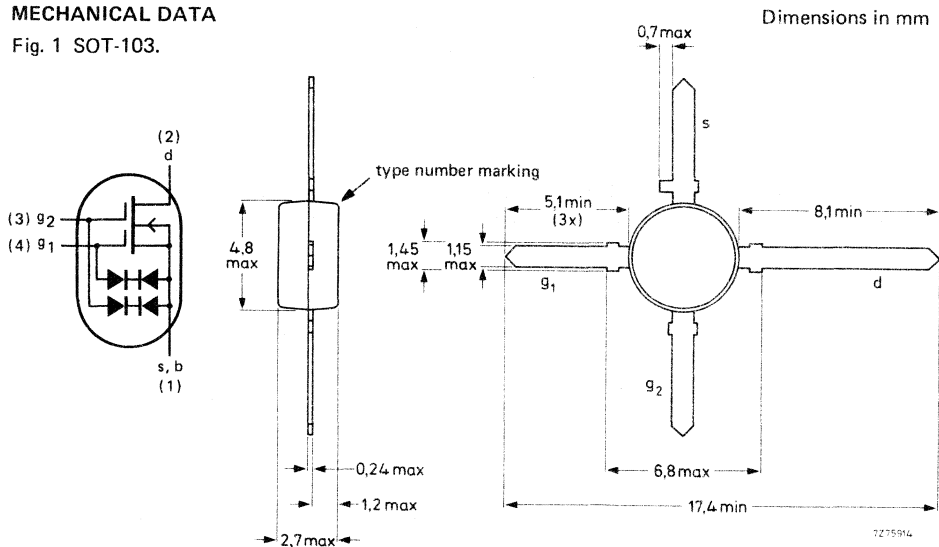
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$ max.	20 V	
Drain current (peak value)	$I_{DM}$ max.	30 mA	
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	$P_{tot}$ max.	225 mW	
Junction temperature	$T_j$ max.	150 $^{\circ}\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ Y_{fs} $ typ.	12 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$ typ.	25 fF	
Noise figure at $G_S = 2\text{ mA/V}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 800\text{ MHz}$	$F$ typ.	2,8 dB	
Power gain at $f = 800\text{ MHz}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V};$ $G_S = 2\text{ mS}; G_L = 1\text{ mS}$	$G_p$ typ.	16,5 dB	←

### MECHANICAL DATA

Fig. 1 SOT-103.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

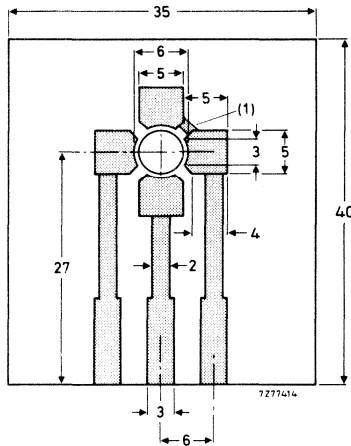
Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	20 mA
Drain current (peak value)	$I_{DM}$	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air  
mounted on the printed-circuit board

$$R_{th\ j-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35  $\mu\text{m}$  Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for  $R_{th}$  measurement.

## STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$   $\pm I_{G1-SS} < 50\text{ nA}$  $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$   $\pm I_{G2-SS} < 50\text{ nA}$ 

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$   $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$  $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$   $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$ 

Drain current\*

 $V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$   $I_{DSS} 2\text{ to }20\text{ mA}$ 

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$   $-V_{(P)G1-S} < 2,7\text{ V}$  $I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$   $-V_{(P)G2-S} < 2,7\text{ V}$ 

## DYNAMIC CHARACTERISTICS

Measuring conditions (common source):  $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at  $f = 1\text{ kHz}$  $|Y_{fs}| > 9,5\text{ mS}$   
typ. 12 mS ←Input capacitance at gate 1;  $f = 1\text{ MHz}$  $C_{ig1-s}$  typ. 1,8 pFInput capacitance at gate 2;  $f = 1\text{ MHz}$  $C_{ig2-s}$  typ. 1,0 pFFeedback capacitance at  $f = 1\text{ MHz}$  $C_{rs}$  typ. 25 fFOutput capacitance at  $f = 1\text{ MHz}$  $C_{os}$  typ. 0,9 pFNoise figure at  $G_S = 2\text{ mA/V}$  $f = 200\text{ MHz}$   $F$  typ. 1,6 dB $f = 800\text{ MHz}$   $F$  typ. 2,8 dBPower gain at  $G_S = 2\text{ mA/V}$  $G_L = 0,5\text{ mS}; f = 200\text{ MHz}$   $G_p$  typ. 23 dB $G_L = 1\text{ mS}; f = 800\text{ MHz}$   $G_p$  typ. 16,5 dB ←

\* Measured under pulse conditions.



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications in television tuners, especially in r.f. stages and mixer stages in S-channel tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

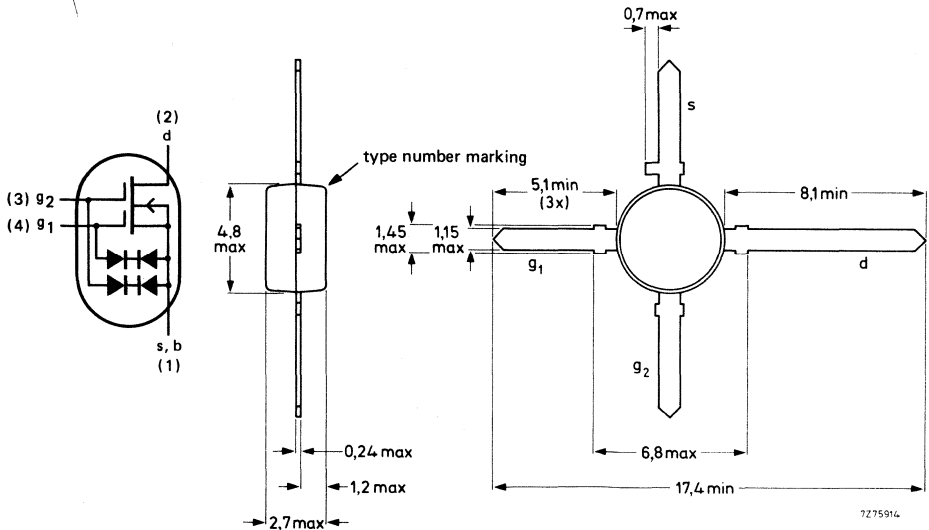
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V	
Drain-current	$I_D$	max.	30 mA	
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW	
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF	
Noise figure at $G_S = 2\text{ mA/V}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	1,5 dB	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



7275914

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

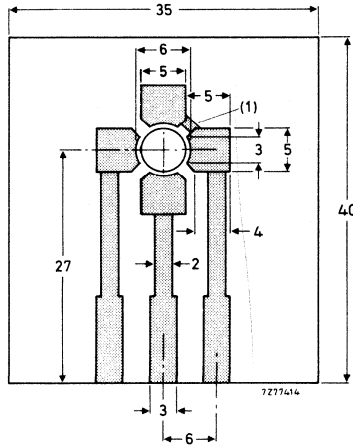
Drain-source voltage	$V_{DS}$	max.	20 V
Drain-current (d.c. or average)	$I_D$	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air  
 mounted on the printed-circuit board (see Fig. 2)

$R_{thj-a} = 335\text{ K/W}$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35  $\mu\text{m}$  Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for  $R_{th}$  measurement.



## STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$   $\pm I_{G1-SS} < 50\text{ nA}$  $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$   $\pm I_{G2-SS} < 50\text{ nA}$ 

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$   $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$  $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$   $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$ 

Drain current\*

 $V_{DS} = 15\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$   $I_{DSS} 2\text{ to }20\text{ mA}$ 

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$   $-V_{(P)G1-S} < 2,5\text{ V}$  $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$   $-V_{(P)G2-S} < 2,0\text{ V}$ 

## DYNAMIC CHARACTERISTICS

Measuring conditions (common source);  $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at  $f = 1\text{ kHz}$  $|Y_{fs}| > 15\text{ mS}$   
typ. 17 mS ←Input capacitance at gate 1;  $f = 1\text{ MHz}$  $C_{ig1-s}$  typ. 2,5 pF  
< 3,0 pFInput capacitance at gate 2;  $f = 1\text{ MHz}$  $C_{ig2-s}$  typ. 1,2 pFFeedback capacitance at  $f = 1\text{ MHz}$  $C_{rs}$  typ. 25 fF  
< 35 fFOutput capacitance at  $f = 1\text{ MHz}$  $C_{os}$  typ. 1,0 pF  
< 1,3 pFNoise figure at  $G_S = 2\text{ mS}$  $f = 200\text{ MHz}$  $F$  typ. 1,5 dB  
< 2,8 dB ←Power gain at  $G_S = 2\text{ mS V}$  $G_L = 0,5\text{ mS}; f = 200\text{ MHz}$  $G_p$  typ. 25 dB ←

\* Measured under pulse conditions.



## SILICON N-CANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

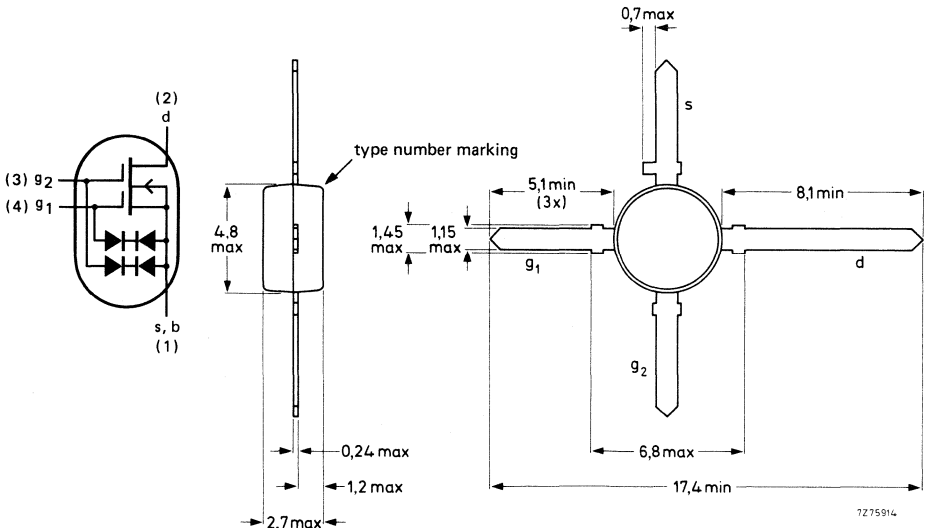
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V	
Drain-current	$I_D$	max.	30 mA	
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW	
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF	
Noise figure at $G_S = 2\text{ mA/V}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; f = 800\text{ MHz}$	F	typ.	2,8 dB	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

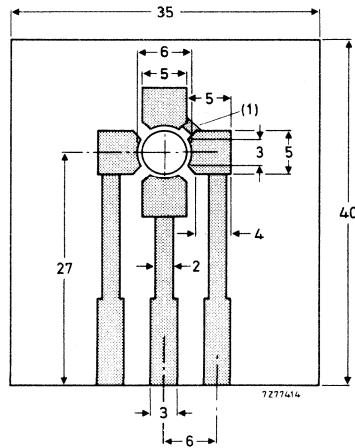
Drain source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air  
 mounted on the printed-circuit board (see Fig. 2)

$R_{thj-a} = 335\text{ K/W}$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35  $\mu\text{m}$  Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for  $R_{th}$  measurement.

## STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$   $\pm I_{G1-SS} < 50\text{ nA}$  $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$   $\pm I_{G2-SS} < 50\text{ nA}$ 

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$   $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$  $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$   $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$ 

Drain current\*

 $V_{DS} = 15\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$   $I_{DSS} 2\text{ to }20\text{ mA}$ 

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$   $-V_{(P)G1-S} < 2,5\text{ V}$  $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$   $-V_{(P)G2-S} < 2,0\text{ V}$ 

## DYNAMIC CHARACTERISTICS

Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at  $f = 1\text{ kHz}$  $|y_{fs}| > 15\text{ mS}$   
typ. 17 mS ←Input capacitance at gate 1;  $f = 1\text{ MHz}$  $C_{ig1-s}$  typ. 2,2 pF  
< 2,6 pFInput capacitance at gate 2;  $f = 1\text{ MHz}$  $C_{ig2-s}$  typ. 1,1 pFFeedback capacitance at  $f = 1\text{ MHz}$  $C_{rs}$  typ. 25 fF  
< 35 fFOutput capacitance at  $f = 1\text{ MHz}$  $C_{os}$  typ. 0,8 pF  
< 1,2 pFNoise figure at  $G_S = 2\text{ mS}$  $f = 200\text{ MHz}$   $F$  typ. 1,5 dB ← $f = 800\text{ MHz}$   $F$  typ. 2,8 dB  
< 3,9 dBPower gain at  $G_S = 2\text{ mS}$  $G_L = 0,5\text{ mS}; f = 200\text{ MHz}$   $G_p$  typ. 25 dB ← $G_L = 1\text{ mS}; f = 800\text{ MHz}$   $G_p$  typ. 18 dB

\* Measured under pulse conditions.



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

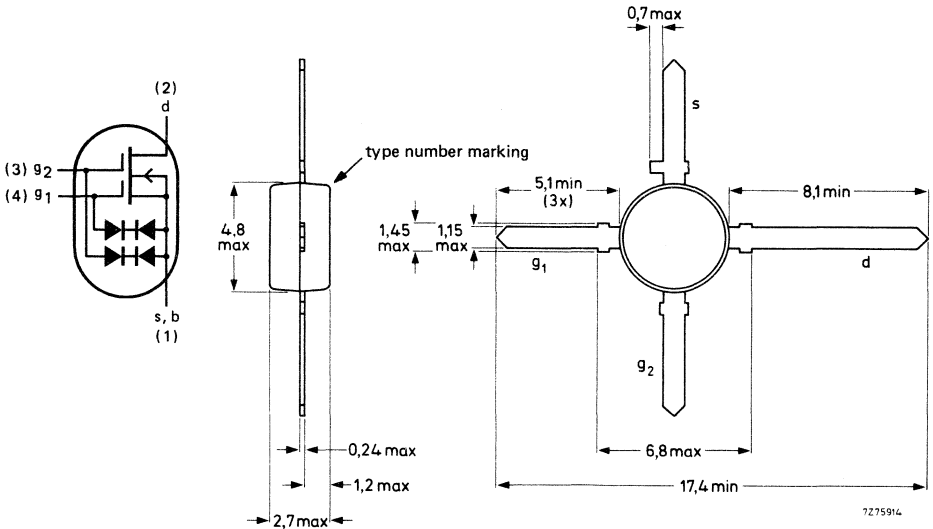
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	18 V	
Drain current	$I_D$	max.	30 mA	
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	225 mW	
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$ ; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	19 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$ ; $+V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF	
Noise figure at $G_S = 5\text{ mS}$ $I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$ ; $+V_{G2-S} = 4\text{ V}$ ; $f = 800\text{ MHz}$	$F$	typ.	2,8 dB	←

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

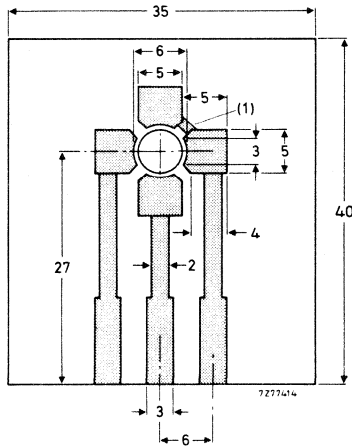
Drain-source voltage	$V_{DS}$	max.	18	V
Drain current (d.c. or average)	$I_D$	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225	mW
Storage temperature	$T_{stg}$	-65 to +150		$^\circ\text{C}$
Junction temperature	$T_j$	max.	150	$^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air  
 mounted on the printed-circuit board (see Fig. 2)

$R_{th\ j-a} = 335\text{ K/W}$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35  $\mu\text{m}$  Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for  $R_{th}$  measurement.



**STATIC CHARACTERISTICS** $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

Gate cut-off currents

 $\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$  $\pm I_{G1-SS} < 25\text{ nA}$  $\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$  $\pm I_{G2-SS} < 25\text{ nA}$ 

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$  $\pm V_{(BR)G1-SS} > 8\text{ V}$  $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$  $\pm V_{(BR)G2-SS} > 8\text{ V}$ 

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$  $-V_{(P)G1-S} < 1,3\text{ V}$  $> 0,2\text{ V}$  $I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$  $-V_{(P)G2-S} < 1,1\text{ V}$  $> 0,2\text{ V}$ **DYNAMIC CHARACTERISTICS**Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at  $f = 1\text{ kHz}$  $|y_{fs}| > 17\text{ mS}$   
typ. 19 mS ←Input capacitance at gate 1;  $f = 1\text{ MHz}$  $C_{ig1-s} < 3,0\text{ pF}$   
typ. 2,6 pFFeedback capacitance at  $f = 1\text{ MHz}$  $C_{rs} < 35\text{ fF}$   
typ. 25 fFOutput capacitance at  $f = 1\text{ MHz}$  $C_{os} < 1,3\text{ pF}$   
typ. 1,1 pFNoise figure at  $f = 800\text{ MHz}; G_S = 5\text{ mS}$  $F < 3,9\text{ dB}$   
typ. 2,8 dB ←



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

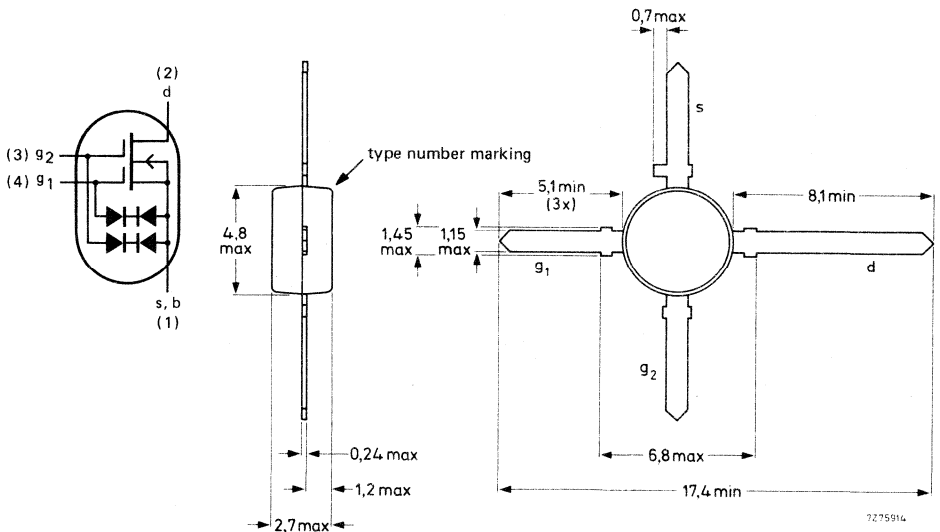
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V	
Drain current	$I_D$	max.	20 mA	
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW	
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$ ; $+V_{G2-S} = 4\text{ V}$	$ Y_{fs} $	typ.	14 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$ ; $+V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	20 fF	
Noise figure at optimum source admittance $I_D = 10\text{ mA}$ ; $V_{DS} = 10\text{ V}$ ; $+V_{G2-S} = 4\text{ V}$ ; $f = 200\text{ MHz}$	F	typ.	0,7 dB	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



**RATINGS**

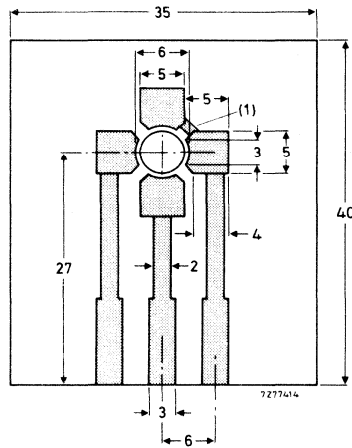
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	20 mA
Drain current (peak value)	$I_{DM}$	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW
Storage temperature	$T_{stg}$	-65 to + 150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air  
 mounted on the printed-circuit board (see Fig. 2)

$R_{th\ j-a} = 335\text{ K/W}$



Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35  $\mu\text{m}$  Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for  $R_{th}$  measurement.

**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Gate cut-off currents

$$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0 \quad \pm I_{G1-SS} < 50\text{ nA}$$

$$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0 \quad \pm I_{G2-SS} < 50\text{ nA}$$

Gate-source breakdown voltages

$$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0 \quad \pm V_{(BR)G1-SS} > 6\text{ V}$$

$$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0 \quad \pm V_{(BR)G2-SS} > 6\text{ V}$$

Drain current

$$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^{\circ}\text{C} \quad I_{DSS} \quad 4\text{ to }25\text{ mA}$$

Gate-source cut-off voltages

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V} \quad -V_{(P)G1-S} < 2,5\text{ V}$$

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0 \quad -V_{(P)G2-S} < 2,5\text{ V}$$

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at  $f = 1\text{ kHz}$   $|Y_{fs}|$   $> 10\text{ mS}$   
typ.  $14\text{ mS}$  ←

Input capacitance at gate 1;  $f = 1\text{ MHz}$   $C_{ig1-s}$  typ.  $2,1\text{ pF}$

Input capacitance at gate 2;  $f = 1\text{ MHz}$   $C_{ig2-s}$  typ.  $1,0\text{ pF}$

Feedback capacitance at  $f = 1\text{ MHz}$   $C_{rs}$  typ.  $20\text{ fF}$

Output capacitance at  $f = 1\text{ MHz}$   $C_{os}$  typ.  $1,1\text{ pF}$

Noise figure at  $f = 100\text{ MHz}; G_S = 1\text{ mS}$   $F$  typ.  $0,7\text{ dB}$   
 $< 1,7\text{ dB}$

Noise figure at  $f = 200\text{ MHz}; G_S = 2\text{ mS}$   $F$  typ.  $1,0\text{ dB}$   
 $< 2,0\text{ dB}$

Transducer gain at  $f = 100\text{ MHz}; G_S = 1\text{ mS}; G_L = 0,5\text{ mS}$   $G_{tr}$  typ.  $29\text{ dB}$

Transducer gain at  $f = 200\text{ MHz}; G_S = 2\text{ mS}; G_L = 0,5\text{ mS}$   $G_{tr}$  typ.  $26\text{ dB}$  ←

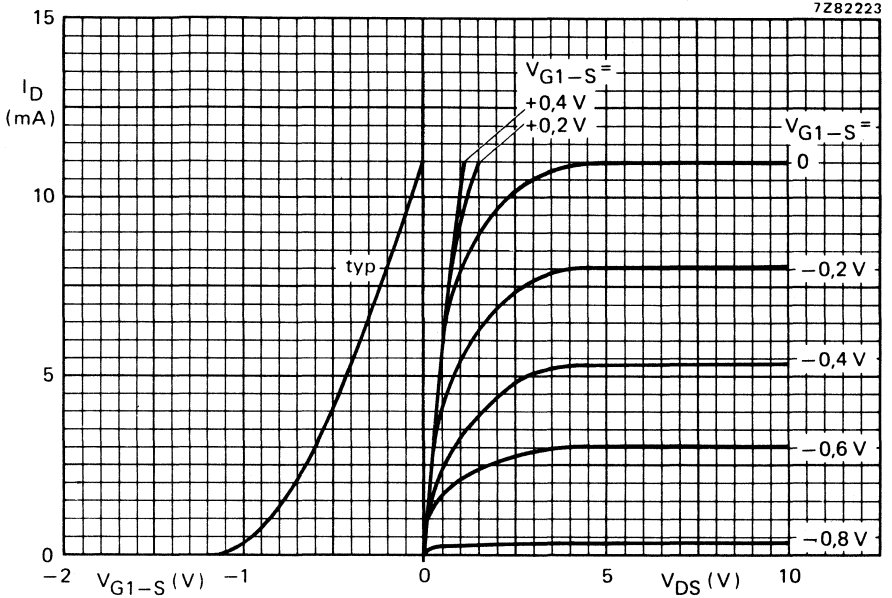


Fig. 3 Left-hand graph:  $V_{DS} = 10\text{ V}$ ;  $V_{G2-S} = +4\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ . Right-hand graph:  $V_{G2-S} = +4\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

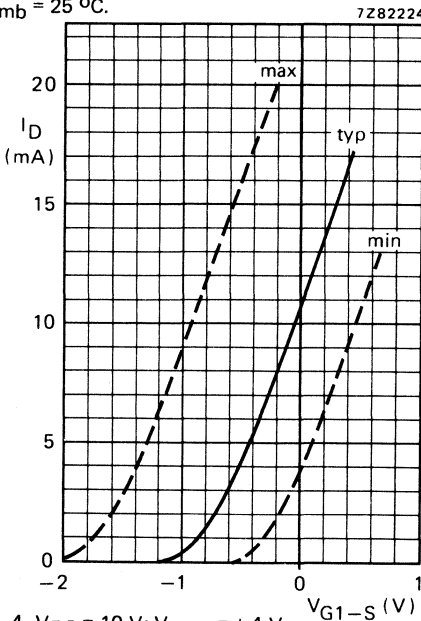


Fig. 4  $V_{DS} = 10\text{ V}$ ;  $V_{G2-S} = +4\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

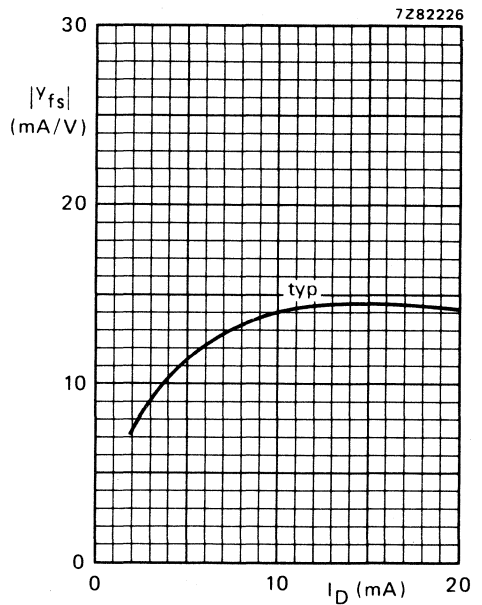


Fig. 5  $V_{DS} = 10\text{ V}$ ;  $V_{G2-S} = +4\text{ V}$ ;  $f = 1\text{ kHz}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

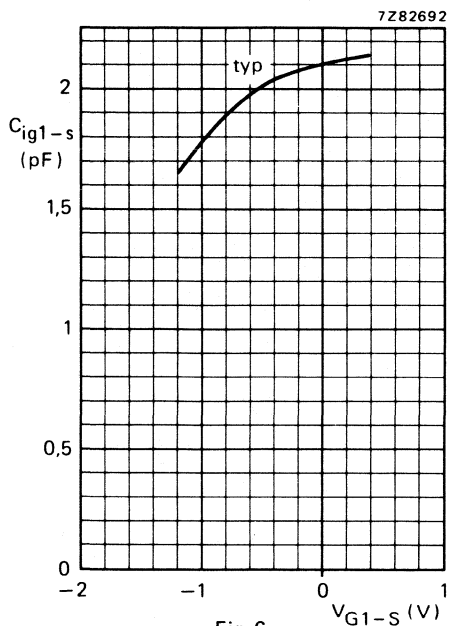


Fig. 6.

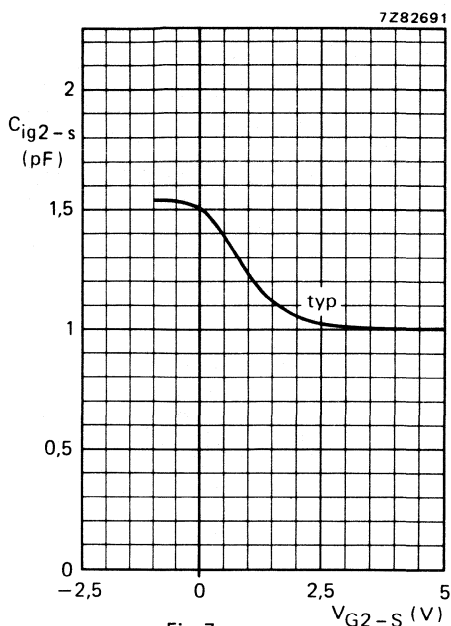


Fig. 7.

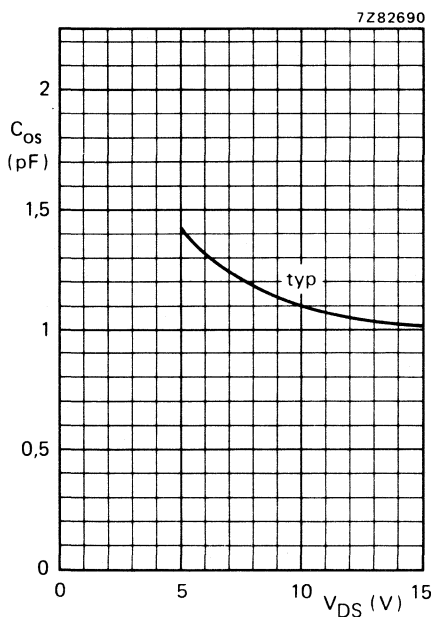


Fig. 8.

## Measuring conditions:

Fig. 6  $V_{DS} = 10$  V;  $V_{G2-S} = +4$  V;  $f = 1$  MHz;  
 $T_{amb} = 25$  °C.

Fig. 7  $V_{DS} = 10$  V;  $V_{G1-S} = 0$ ;  $f = 1$  MHz;  
 $T_{amb} = 25$  °C.

Fig. 8  $V_{G2-S} = +4$  V;  $I_D = 10$  mA;  $f = 1$  MHz;  
 $T_{amb} = 25$  °C.

Measuring conditions for Figs 9 to 12:  $V_{DS} = 10 \text{ V}$ ;  $I_D = 10 \text{ mA}$ ;  $V_{G2-S} = +4 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

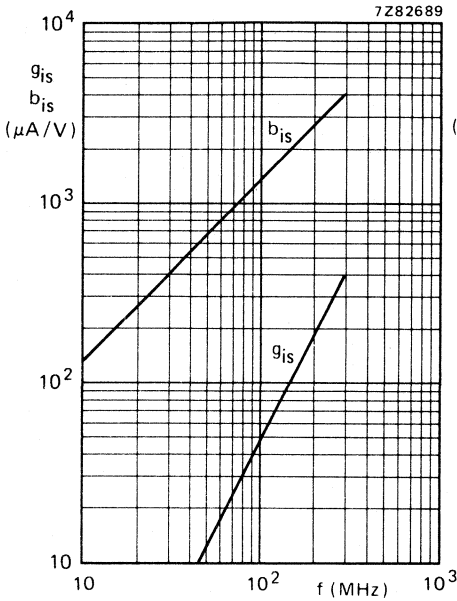


Fig. 9.

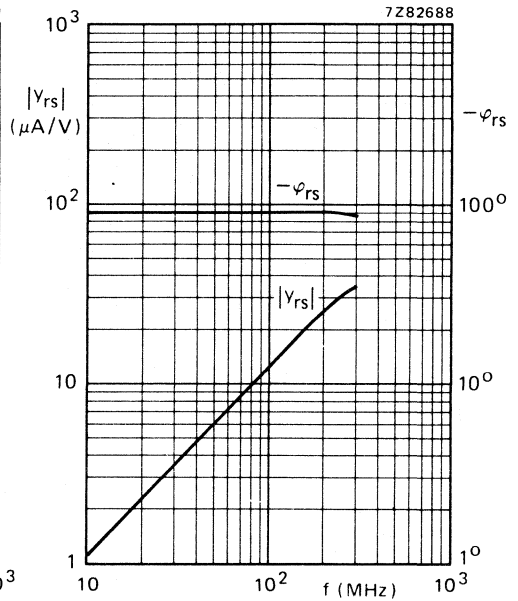


Fig. 10.

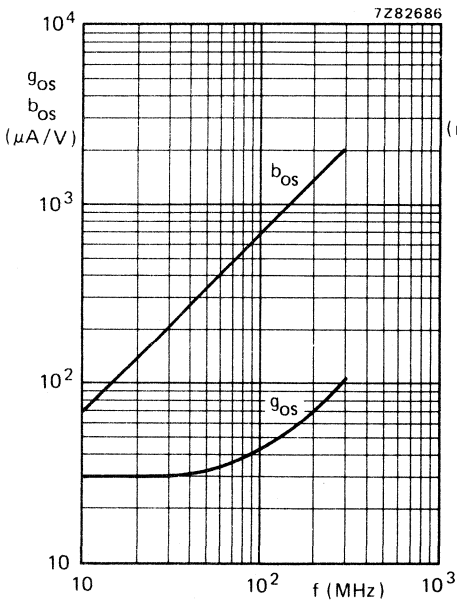


Fig. 11.

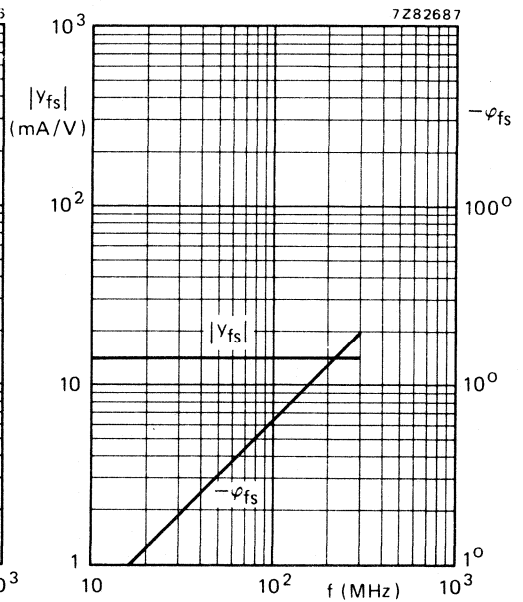


Fig. 12.



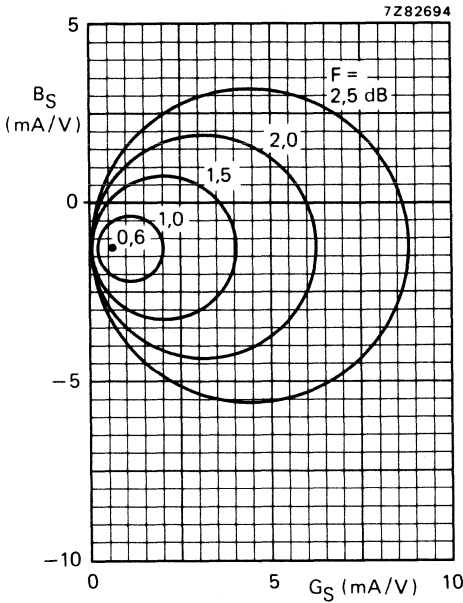


Fig. 13  $V_{DS} = 10 \text{ V}$ ;  $V_{G2-S} = +4 \text{ V}$ ;  $I_D = 10 \text{ mA}$ ;  $f = 100 \text{ MHz}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; circles of typical constant noise figures.

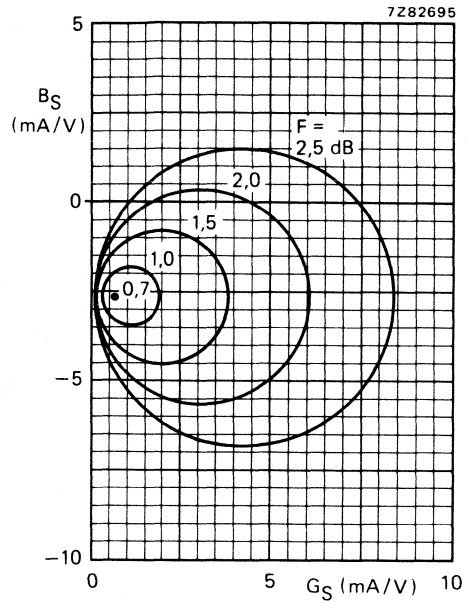


Fig. 14  $V_{DS} = 10 \text{ V}$ ;  $V_{G2-S} = +4 \text{ V}$ ;  $I_D = 10 \text{ mA}$ ;  $f = 200 \text{ MHz}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; circles of typical constant noise figures.

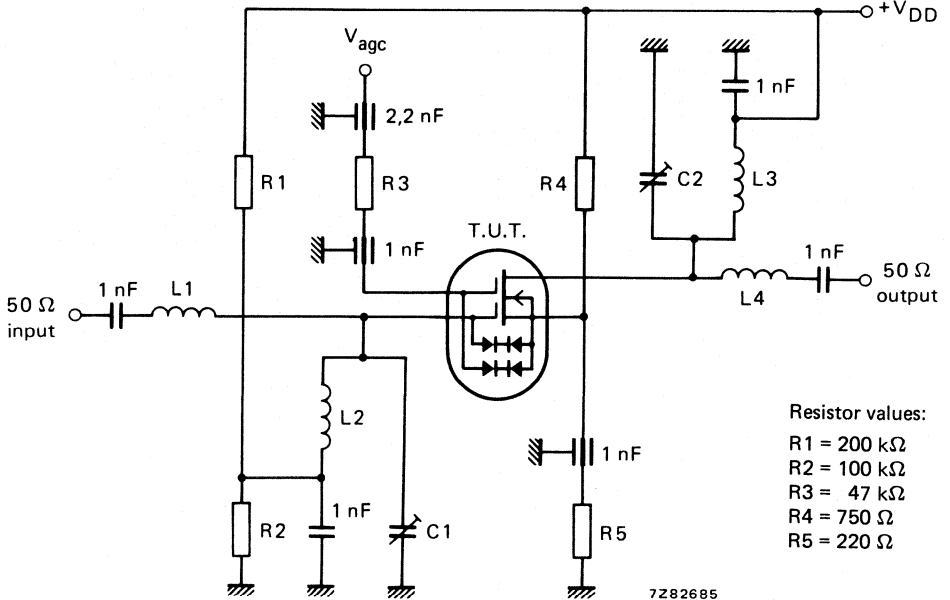


Fig. 15 Automatic gain control test circuit at  $f = 200$  MHz (see also Fig. 16).  
 $V_{DD} = 16$  V;  $G_S = 2$  mA/V;  $G_L = 0,5$  mA/V.

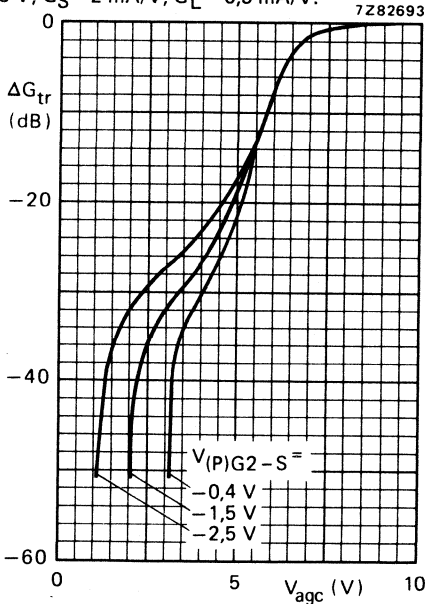


Fig. 16  $V_{DD} = 16$  V;  $f = 200$  MHz;  
 $T_{amb} = 25$  °C; typical values;  
 see also Fig. 15.

## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

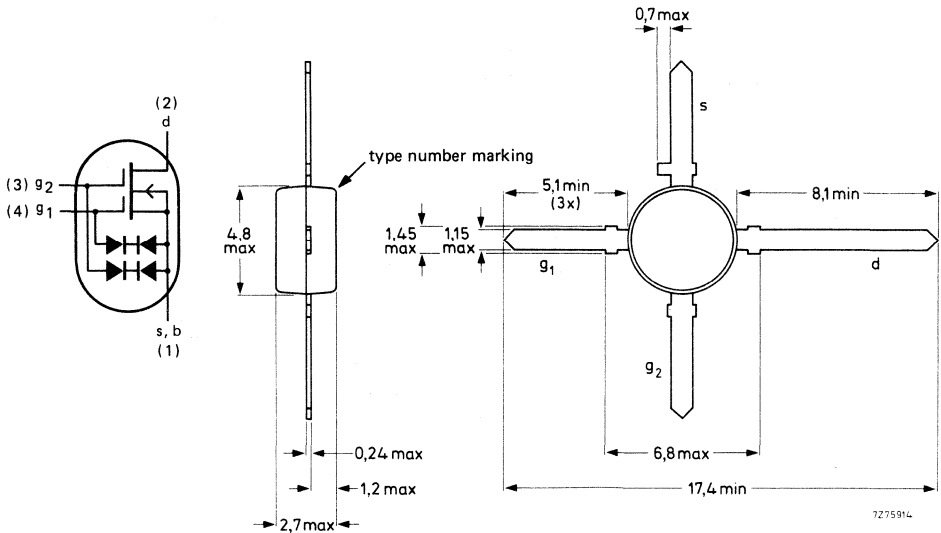
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V	
Drain current	$I_D$	max.	40 mA	
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW	
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	25 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	30 fF	
Noise figure at $G_S = 2\text{ mA/V}$ $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	1,2 dB	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

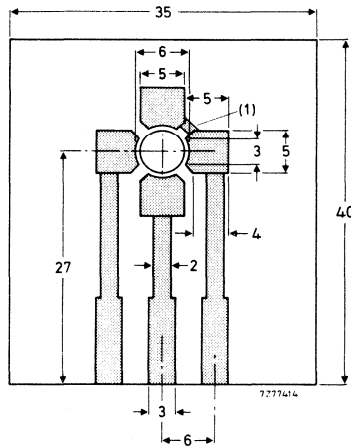
Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^\circ\text{C}$	$P_{tot}$	max.	225 mW
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air  
 mounted on the printed-circuit board (see Fig. 2)

$R_{th\ j-a} = 335\text{ K/W}$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35  $\mu\text{m}$  Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for  $R_{th}$  measurement.

**STATIC CHARACTERISTICS** $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

Gate cut-off currents

$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	8 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	8 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	1,3 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	1,1 V

**DYNAMIC CHARACTERISTICS**Measuring conditions (common source):  $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ 

Transfer admittance at $f = 1\text{ kHz}$	$ y_{fs} $	>	20 mS	←
		typ.	25 mS	
Input capacitance at gate 1; $f = 1\text{ MHz}$	$C_{ig1-s}$	typ.	4,0 pF	
Input capacitance at gate 2; $f = 1\text{ MHz}$	$C_{ig2-s}$	typ.	1,7 pF	
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	typ.	30 fF	
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	typ.	2,0 pF	
Noise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}$	F	typ.	1,2 dB	←



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

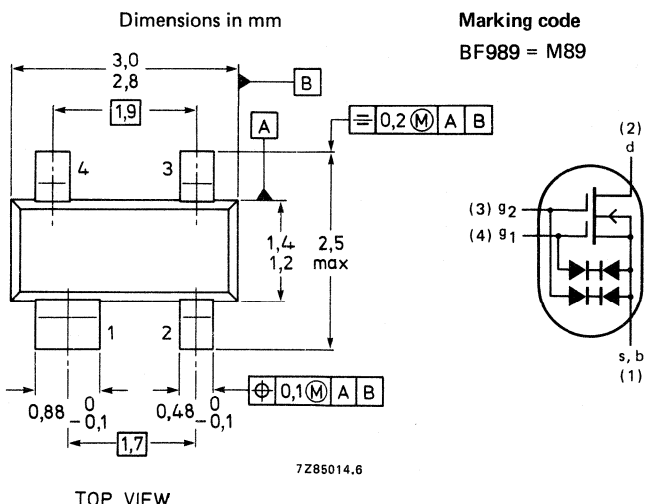
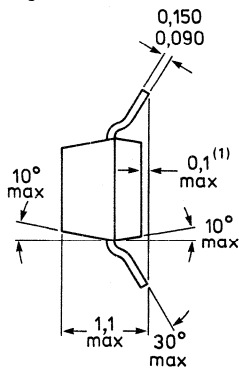
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (peak value)	$I_{DM}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	200 mW
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ Y_{fs} $	typ.	12 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$ $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 800\text{ MHz}$	F	typ.	2,8 dB

### MECHANICAL DATA

Fig. 1 SOT-143.



(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	20 mA
Drain current (peak value)	$I_{DM}$	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50 nA

Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^\circ\text{C}$	$I_{DSS}$		2 to 20 mA
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Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	2,7 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,7 V

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$

→ Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	9,5 mS
		typ.	12 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	$C_{ig1-s}$	typ.	1,8 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	$C_{ig2-s}$	typ.	1,0 pF
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	typ.	25 fF
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	typ.	0,9 pF
→ Noise figure at $G_S = 2\text{ mS}$			
$f = 200\text{ MHz}$	F	typ.	1,6 dB
$f = 800\text{ MHz}$	F	typ.	2,8 dB

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	18 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	200 mW
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	19 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 800\text{ MHz}$	F	typ.	2,8 dB

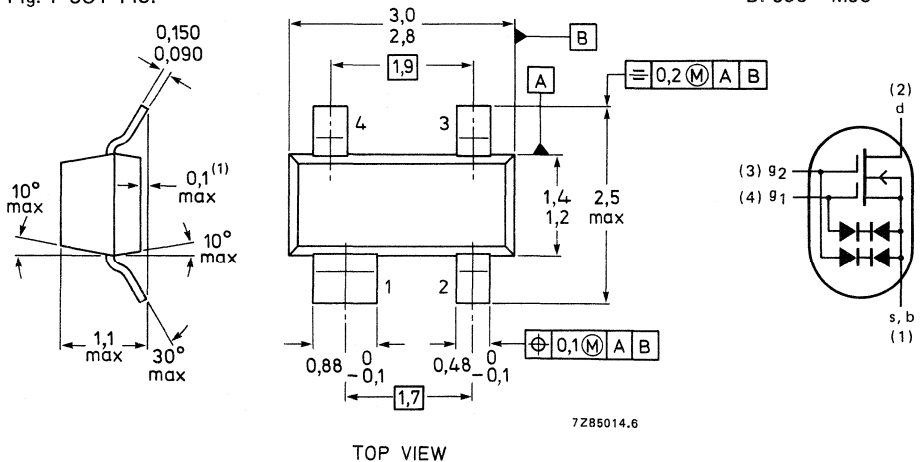
### MECHANICAL DATA

Fig. 1 SOT-143.

Dimensions in mm

Marking code

BF990 = M90



(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	18 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1 source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to +150 $^{\circ}\text{C}$
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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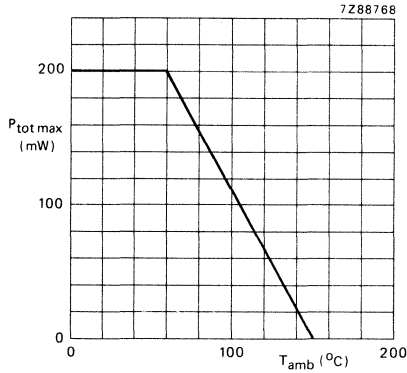


Fig. 2 Power derating curve.

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Gate cut-off currents

gate 1;

$$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$$

$$\pm I_{G1-SS} < 25\text{ nA}$$

gate 2;

$$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$$

$$\pm I_{G2-SS} < 25\text{ nA}$$

Gate-source breakdown voltages

gate 1;

$$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$$

$$\pm V_{(BR)G1-SS} > 8\text{ V}$$

gate 2;

$$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$$

$$\pm V_{(BR)G2-SS} > 8\text{ V}$$

Gate-source cut-off voltages

gate 1;

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$$

$$-V_{(P)G1-S} < 1,3\text{ V}$$

gate 2;

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$$

$$-V_{(P)G2-S} < 1,1\text{ V}$$

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at  $f = 1\text{ kHz}$

$$|y_{fs}| > 17\text{ mS} \leftarrow$$

typ. 19 mS

Input capacitance at gate 1;  $f = 1\text{ MHz}$

$$C_{ig1-s} \text{ typ. } 3\text{ pF}$$

Input capacitance at gate 2;  $f = 1\text{ MHz}$

$$C_{ig2-s} \text{ typ. } 2,6\text{ pF} \leftarrow$$

Feedback capacitance at  $f = 1\text{ MHz}$

$$C_{rs} \text{ typ. } 25\text{ fF}$$

Output capacitance at  $f = 1\text{ MHz}$

$$C_{os} \text{ typ. } 1,2\text{ pF}$$

Noise figure at  $f = 800\text{ MHz}; G_S = 5\text{ mS}$

$$F \text{ typ. } 2,8\text{ dB} \leftarrow$$



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

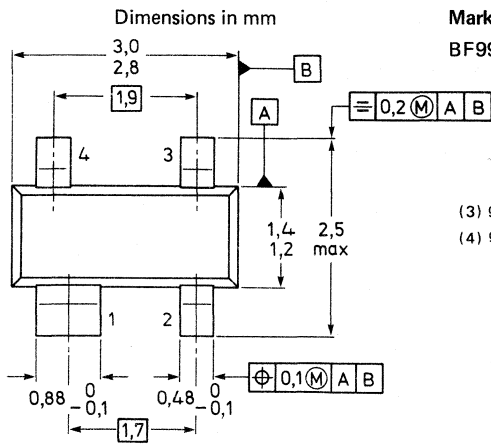
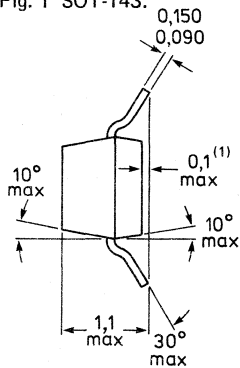
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

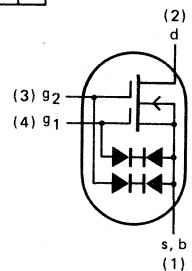
Drain-source voltage	$V_{DS}$	max.	20 V	
Drain current	$I_D$	max.	20 mA	
Total power dissipation up to $T_{amb} = 60\text{ }^\circ\text{C}$	$P_{tot}$	max.	200 mW	
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ Y_{fs} $	typ.	14 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	20 fF	
Noise figure at optimum source admittance $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	0,7 dB	

### MECHANICAL DATA

Fig. 1 SOT-143.



Marking code  
BF991 = M91



TOP VIEW

(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	20 mA
Drain current (peak value)	$I_{DM}$	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50 nA

Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^\circ\text{C}$	$I_{DSS}$		4 to 25 mA
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Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	6 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	6 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	2,5 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,5 V

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$

→ Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	10 mS
		typ.	14 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	$C_{ig1-s}$	typ.	2,1 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	$C_{ig2-s}$	typ.	1,0 pF
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	typ.	20 fF
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	typ.	1,1 pF
→ Noise figure			
$f = 100\text{ MHz}; G_S = 1\text{ mS}$	F	typ.	0,7 dB
		<	1,7 dB
$f = 200\text{ MHz}; G_S = 2\text{ mS}$	F	typ.	1,0 dB
		<	2,0 dB
→ Transducer gain **			
$f = 100\text{ MHz}; G_S = 1\text{ mS}; G_L = 0,5\text{ mS}$	$G_{tr}$	typ.	29 dB
$f = 200\text{ MHz}; G_S = 2\text{ mS}; G_L = 0,5\text{ mS}$	$G_{tr}$	typ.	26 dB

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

\*\* Crystal mounted in a SOT-103 envelope.

## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

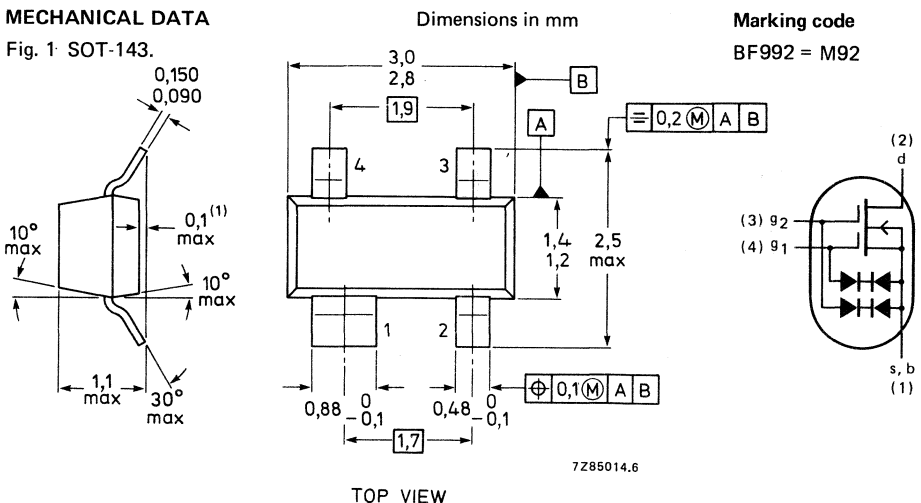
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current	$I_D$	max.	40 mA
Total power dissipation up to $T_{amb} = 60\text{ }^\circ\text{C}$	$P_{tot}$	max.	200 mW
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	25 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	30 fF
Noise figure at $G_S = 2\text{ mS}$ $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	1,2 dB

### MECHANICAL DATA

Fig. 1: SOT-143.



**Marking code**  
BF992 = M92

(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (d.c. or average)	$I_D$	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		$-65\text{ to }+150\text{ }^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	8 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	8 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$		0,2 to 1,3 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$		0,2 to 1,1 V

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$

→ Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	20 mS
		typ.	25 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	$C_{ig1-s}$	typ.	4 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	$C_{ig2-s}$	typ.	1,7 pF
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	typ.	30 fF
		<	40 fF
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	typ.	2 pF
→ Noise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}$	F	typ.	1,2 dB

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

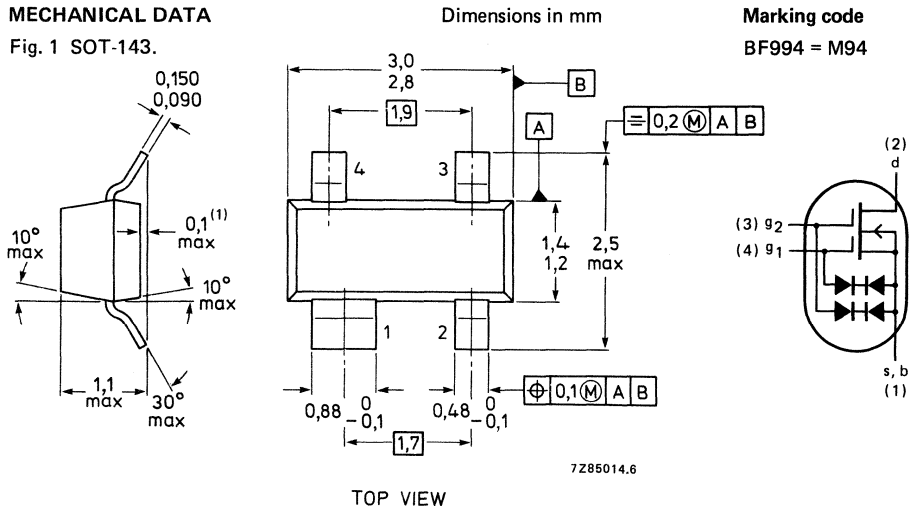
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	200 mW
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	1,5 dB

### MECHANICAL DATA

Fig. 1 SOT-143.



(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1 source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to + 150 $^{\circ}\text{C}$
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{thj-a}$	=	460 K/W
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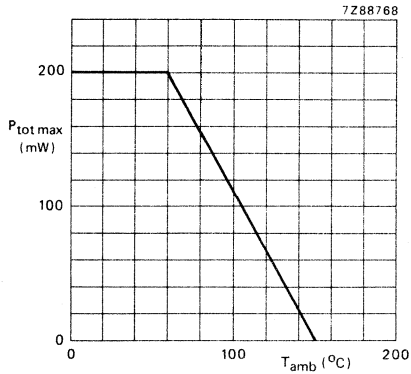


Fig. 2 Power derating curve.

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

**STATIC CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

## Gate cut-off currents

gate 1;

$$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0 \quad \pm I_{G1-SS} < 50\text{ nA}$$

gate 2;

$$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0 \quad \pm I_{G2-SS} < 50\text{ nA}$$

## Gate-source breakdown voltages

gate 1;

$$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0 \quad \pm V_{(BR)G1-SS} \quad 6\text{ to }20\text{ V}$$

gate 2;

$$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0 \quad \pm V_{(BR)G2-SS} \quad 6\text{ to }20\text{ V}$$

## Gate-source cut-off voltages

gate 1;

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V} \quad -V_{(P)G1-S} < 2,5\text{ V}$$

gate 2;

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0 \quad -V_{(P)G2-S} < 2,0\text{ V}$$

## Drain-source cut-off voltage

$$V_{DS} = 15\text{ V}; V_{G2-S} = 4\text{ V} \quad I_{DSS} \quad 2\text{ to }20\text{ mA}$$

**DYNAMIC CHARACTERISTICS**

Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at  $f = 1\text{ kHz}$

$$|y_{fs}| \quad > \quad 15\text{ mS} \quad \leftarrow$$

$$\text{typ.} \quad 17\text{ mS}$$

Input capacitance at gate 1;  $f = 1\text{ MHz}$

$$C_{ig1-s} \quad \text{typ.} \quad 2,5\text{ pF}$$

Input capacitance at gate 2;  $f = 1\text{ MHz}$

$$C_{ig2-s} \quad \text{typ.} \quad 1,2\text{ pF}$$

Feedback capacitance at  $f = 1\text{ MHz}$

$$C_{rs} \quad \text{typ.} \quad 25\text{ fF}$$

Output capacitance at  $f = 1\text{ MHz}$

$$C_{os} \quad \text{typ.} \quad 1,0\text{ pF}$$

Noise figure at  $f = 200\text{ MHz}; G_S = 2\text{ mS}$

$$F \quad \text{typ.} \quad 1,5\text{ dB} \quad \leftarrow$$

$$< \quad 2,8\text{ dB}$$

Power gain at  $G_S = 2\text{ mS}$

$$G_L = 0,5\text{ mS}, f = 200\text{ MHz} \quad G_p \quad \text{typ.} \quad 25\text{ dB} \quad \leftarrow$$



## SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope, with source and substrate interconnected, intended for u.h.f. applications, such as television tuners and professional communication equipment.

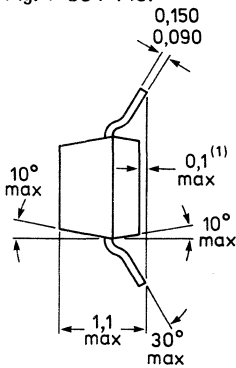
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

### QUICK REFERENCE DATA

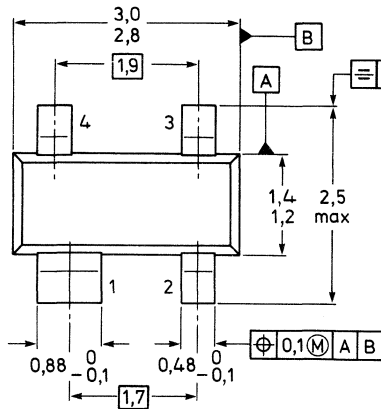
Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	200 mW
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	25 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 800\text{ MHz}$	F	typ.	2,8 dB
$I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	1,5 dB

### MECHANICAL DATA

Fig. 1 SOT-143.

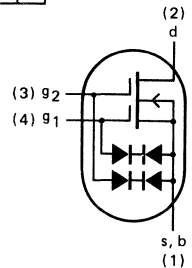


Dimensions in mm



Marking code

BF996 = M96



7285014.6

TOP VIEW

(1) Also available in 0,1 – 0,2 mm version.

See also *Soldering recommendations*.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1 source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to +150 $^{\circ}\text{C}$
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air\*  $R_{thj-a} = 460\text{ K/W}$

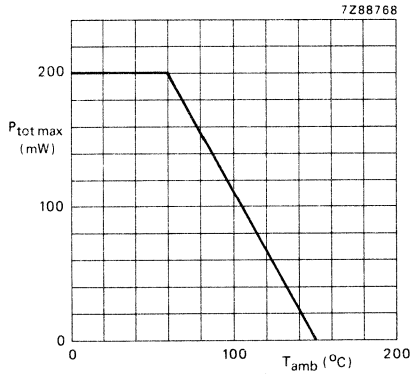


Fig. 2 Power derating curve.

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

**STATIC CHARACTERISTICS** $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Gate cut-off currents

gate 1;

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$   $\pm I_{G1-SS} < 50\text{ nA}$ 

gate 2;

 $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$   $\pm I_{G2-SS} < 50\text{ nA}$ 

Gate-source breakdown voltages

gate 1;

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$   $\pm V_{(BR)G1-SS} 6\text{ to }20\text{ V}$ 

gate 2;

 $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$   $\pm V_{(BR)G2-SS} 6\text{ to }20\text{ V}$ 

Gate-source cut-off voltages

gate 1;

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$   $-V_{(P)G1-S} < 2,5\text{ V}$ 

gate 2;

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$   $-V_{(P)G2-S} < 2,0\text{ V}$ 

Drain-source cut-off voltage

 $V_{DS} = 15\text{ V}; V_{G2-S} = 4\text{ V}$   $I_{DSS} 2\text{ to }20\text{ mA}$ **DYNAMIC CHARACTERISTICS**Measuring conditions (common source):  $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at  $f = 1\text{ kHz}$  $|y_{fs}| > 15\text{ mS}$   
typ. 17 mS ←Input capacitance at gate 1;  $f = 1\text{ MHz}$  $C_{ig1-s}$  typ. 2,2 pFInput capacitance at gate 2;  $f = 1\text{ MHz}$  $C_{ig2-s}$  typ. 1,1 pFFeedback capacitance at  $f = 1\text{ MHz}$  $C_{rs}$  typ. 25 fFOutput capacitance at  $f = 1\text{ MHz}$  $C_{os}$  typ. 0,8 pF

Noise figure

at  $G_S = 2\text{ mS}, f = 200\text{ MHz}$ 

F typ. 1,5 dB ←

at  $G_S = 2\text{ mS}, f = 800\text{ MHz}$ F typ. 2,8 dB  
< 3,9 dB ←

Power gain

 $G_S = 2\text{ mS}, G_L = 0,5\text{ mS}, f = 200\text{ MHz}$  $G_p$  typ. 25 dB ← $G_S = 2\text{ mS}, G_L = 1,0\text{ mS}, f = 800\text{ MHz}$  $G_p$  typ. 18 dB ←





## N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i. f. and v. h. f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

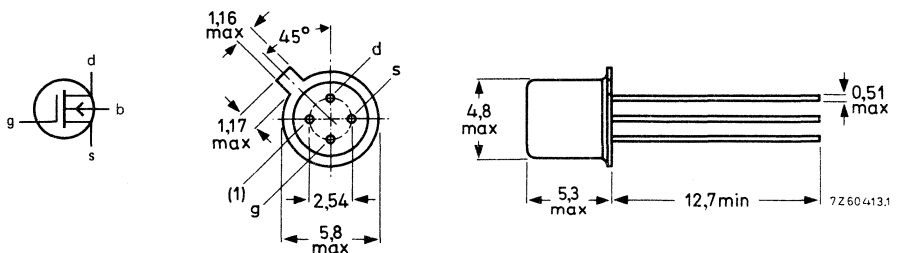
### QUICK REFERENCE DATA

Drain-substrate voltage	$V_{DB}$	max.	30 V	
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V	
Drain current $V_{DS} = 15 \text{ V}; V_{GS} = 0$	$I_{DSS}$		10 to 40 mA	
Transfer admittance $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; f = 1 \text{ kHz}$	$ Y_{fs} $	>	6 mS	←
Feedback capacitance $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz}$	$C_{rs}$	<	0,7 pF	
Noise figure at $f = 200 \text{ MHz}$ $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$ $G_S = 1 \text{ mS}; B_S = B_{Sopt}$	F	<	5 dB	←
Equivalent noise voltage at $f = 1 \text{ kHz}$ $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	$V_n/\sqrt{B}$	typ.	100 nV/ $\sqrt{\text{Hz}}$	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = substrate (b) connected to case

Accessories: 56246 (distance disc).

#### Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	$V_{DB}$	max.	30 V
Source-substrate voltage	$V_{SB}$	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0; f > 100 \text{ Hz}$	$V_{G-N}$	max.	15 V
		min.	-15 V
Drain current (d.c.)	$I_D$	max.	20 mA
Drain current (peak value) $t_p = 20 \text{ ms}; \delta = 0,1$	$I_{DM}$	max.	50 mA
Total power dissipation up to $T_{amb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	200 mW
Storage temperature	$T_{stg}$		-65 to + 125 $^\circ\text{C}$
Junction temperature	$T_j$	max.	125 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air	$R_{th j-a}$	=	500 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Gate currents;  $V_{BS} = 0$

$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10\text{ V}; V_{DS} = 0$	$I_{GSS}$	<	10	pA
$-V_{GS} = 10\text{ V}; V_{DS} = 0; T_j = 125\text{ }^\circ\text{C}$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10\text{ V}; V_{DS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{GSS}$	<	200	pA

Bulk currents;  $V_{GB} = 0$

$-V_{BD} = 30\text{ V}; I_S = 0$	$-I_{BDO}$	<	10	$\mu\text{A}$
$-V_{BS} = 30\text{ V}; I_D = 0$	$-I_{BSO}$	<	10	$\mu\text{A}$

Drain current

$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	10 to 40	mA
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Gate-source voltage

$I_D = 100\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{GS}$	0.5 to 3.5	V
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Gate-source cut-off voltage

$I_D = 100\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	<	4	V
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y parameters  $T_{amb} = 25\text{ }^\circ\text{C}$

$I_D = 5\text{ mA}; V_{DS} = 15\text{ V}$				
Transfer admittance at $f = 1\text{ kHz}$	$ y_{fs} $	>	6	mS ←
Output admittance at $f = 1\text{ kHz}$	$ y_{os} $	<	0.4	mS
Input capacitance at $f = 1\text{ MHz}$	$C_{is}$	<	5	pF
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	<	0.7	pF
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	<	3	pF

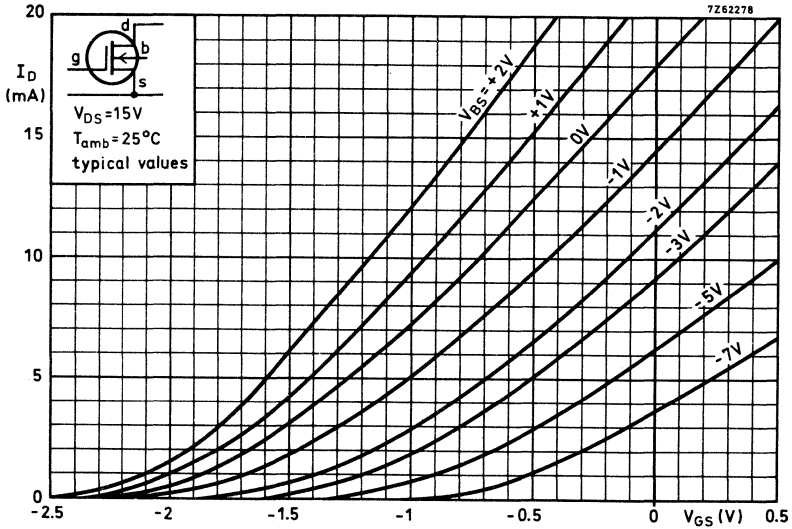
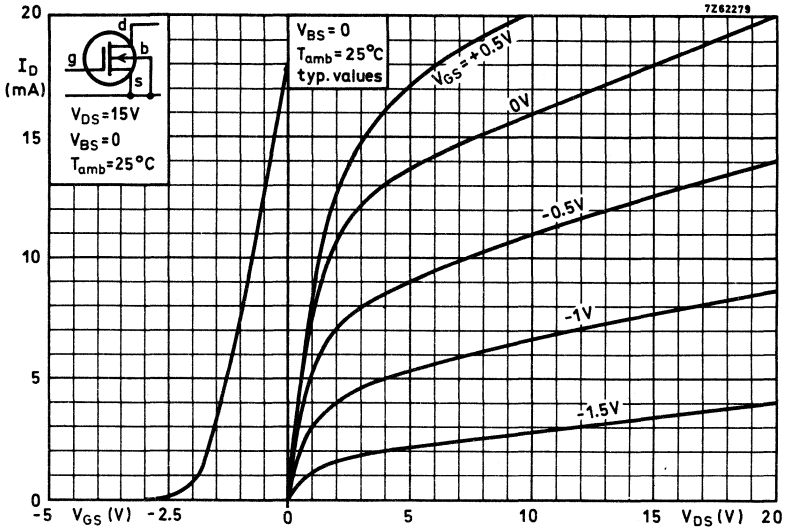
Noise figure at  $f = 200\text{ MHz}$   $T_{amb} = 25\text{ }^\circ\text{C}$

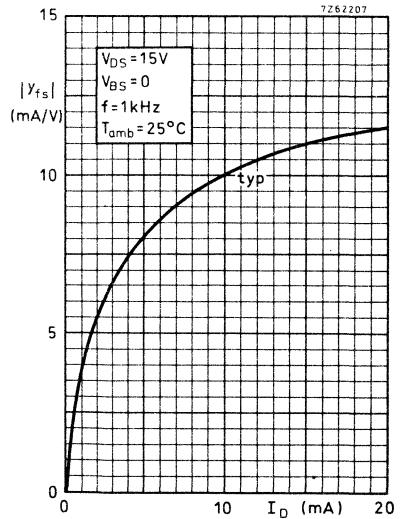
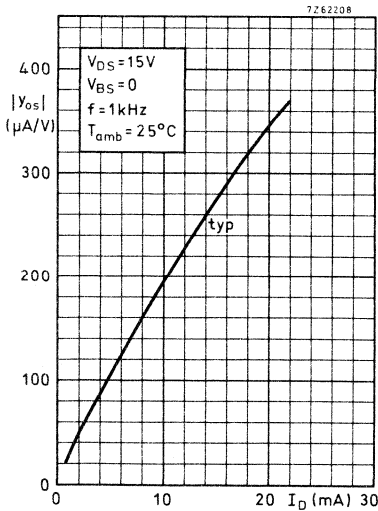
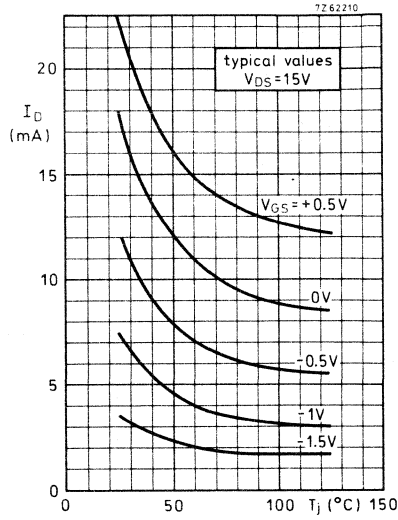
$I_D = 5\text{ mA}; V_{DS} = 15\text{ V}$				
$G_S = 1\text{ mS}; B_S = B_{Sopt}$	F	<	5	dB ←

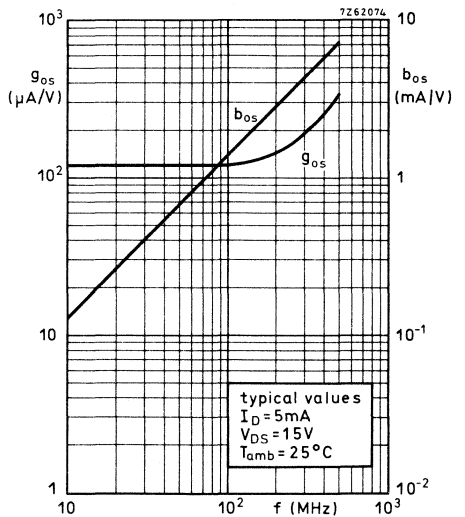
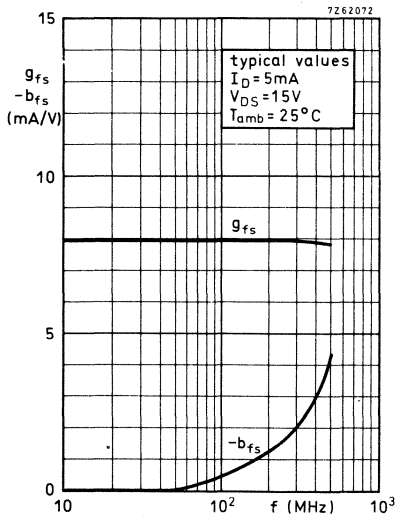
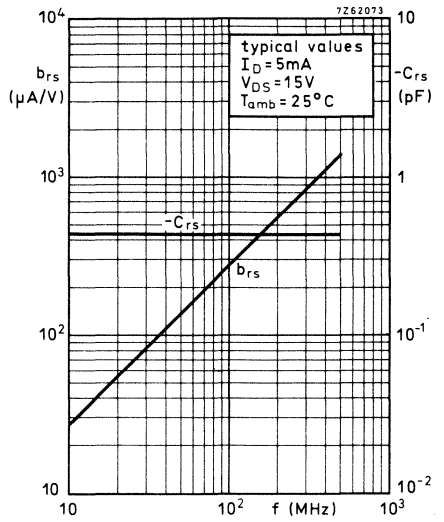
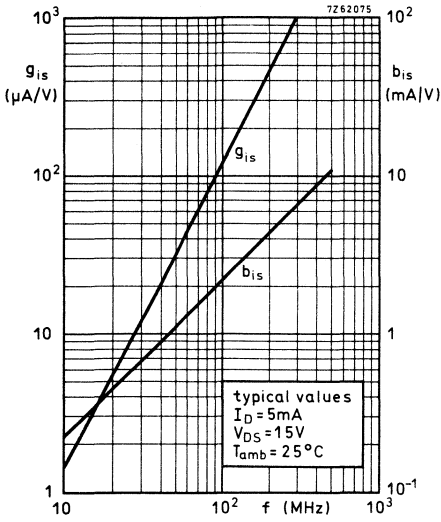
Equivalent noise voltage  $T_{amb} = 25\text{ }^\circ\text{C}$

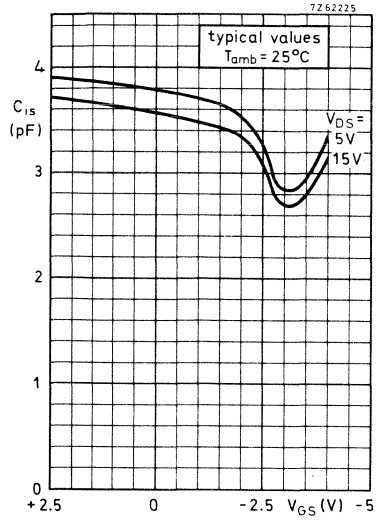
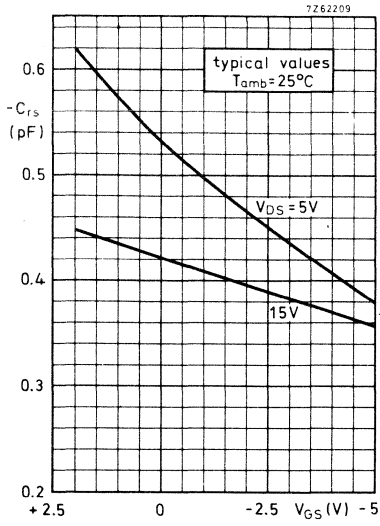
$I_D = 5\text{ mA}; V_{DS} = 15\text{ V}; f = 120\text{ Hz}$	$V_n/\sqrt{B}$	typ.	300	$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{ kHz}$	$V_n/\sqrt{B}$	typ.	100	$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{ kHz}$	$V_n/\sqrt{B}$	typ.	35	$\text{nV}/\sqrt{\text{Hz}}$

# BFR29













## SILICON N-CHANNEL DUAL IG-MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

**This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.**

The tetrode configuration, a series arrangement of two gate controlled channels, offers:

- very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
- excellent signal handling capability over the entire gain control range.
- low noise figure combined with high gain.

### QUICK REFERENCE DATA

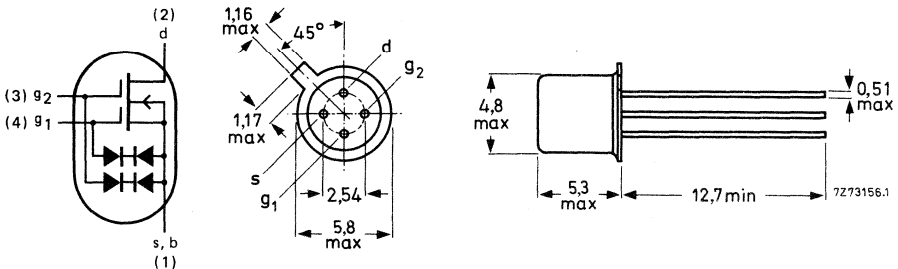
Drain-source voltage	$V_{DS}$	max.	20 V	
Drain current	$I_D$	max.	50 mA	
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW	
Junction temperature	$T_j$	max.	175 $^\circ\text{C}$	
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ Y_{fs} $	typ.	15 mS	←
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$C_{rs}$	typ.	30 fF	
Noise figure at optimum source admittance $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$ $G_S = 1,2\text{ mS}; -B_S = 5,7\text{ mS}; f = 200\text{ MHz}$	F	typ.	2,3 dB	←

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

Source and substrate connected to the case.



Accessories: 56246 (distance disc).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20	V
Drain current (d. c. or average)	$I_D$	max.	50	mA
Drain current (peak value)	$I_{DM}$	max.	100	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300	mW
Storage temperature	$T_{stg}$	-65 to +175	$^\circ\text{C}$	
Junction temperature	$T_j$	max.	175	$^\circ\text{C}$

**THERMAL RESISTANCE**

→ From junction to ambient in free air  $R_{th\ j-a} = 0,5\text{ K/mW}$

## STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

## Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	10	nA
$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$	$\pm I_{G1-SS}$	<	10	$\mu\text{A}$
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	10	nA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$	$\pm I_{G2-SS}$	<	10	$\mu\text{A}$

## Gate-source breakdown voltages

$\pm I_{G1-SS} = 0,1\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	6,0 to 20	V
$\pm I_{G2-SS} = 0,1\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	6,0 to 20	V

## Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$	$I_{DSS}$	20 to 55	mA <sup>1)</sup>
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## Gate 1-source voltage

$I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{G1-S}$	0,6 to 2,1	V
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## Gate-source cut-off voltages

$I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	1,5 to 3,8	V
$I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	1,5 to 3,4	V

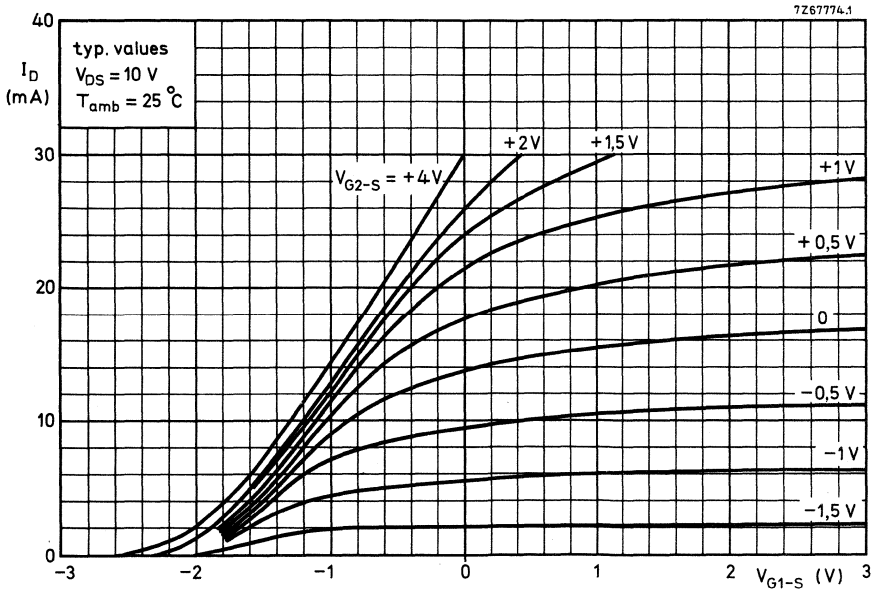
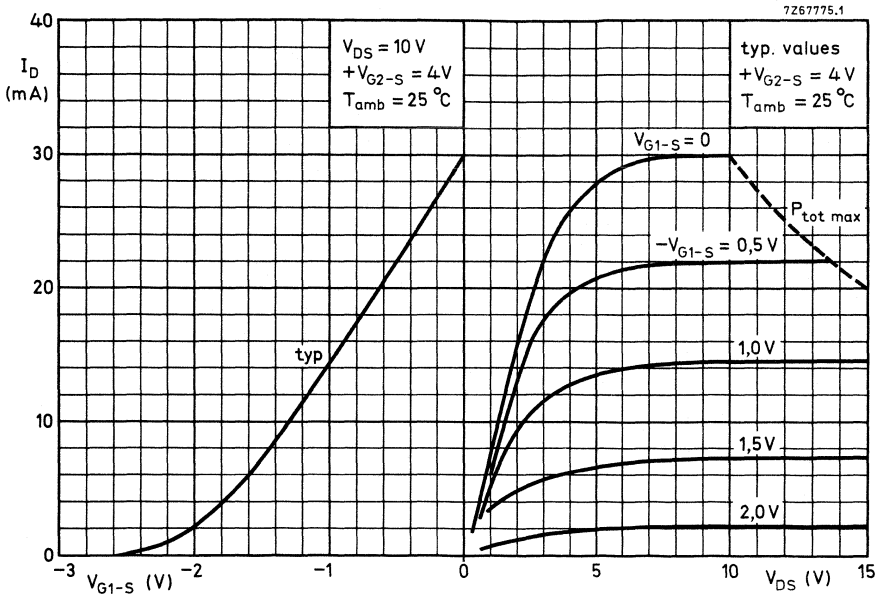
<sup>1)</sup> Measured under pulse conditions.

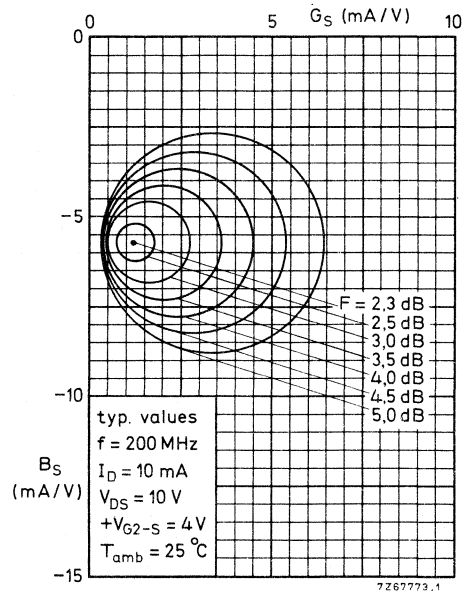
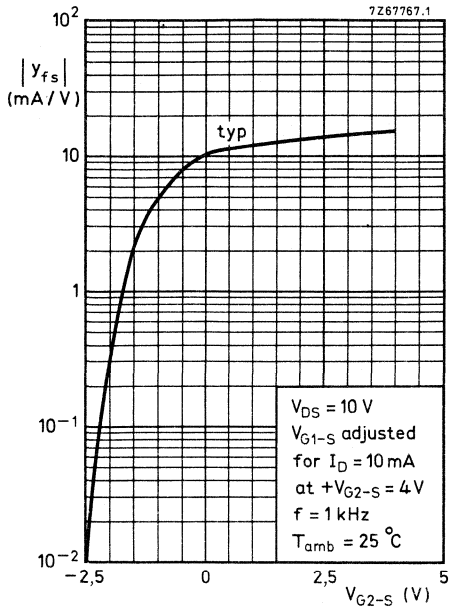
## DYNAMIC CHARACTERISTICS

Measuring conditions (common source):  $I_D = 10 \text{ mA}$ ;  $V_{DS} = 10 \text{ V}$ ;  $+V_{G2-S} = 4 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

→	Transfer admittance at $f = 1 \text{ kHz}$	$ y_{fs} $	>	12	mS
			typ.	15	mS
	Input capacitance at $f = 1 \text{ MHz}$	$C_{is}$	typ.	5,5	pF
	Feedback capacitance at $f = 1 \text{ MHz}$	$C_{rs}$	typ.	30	fF
	Output capacitance at $f = 1 \text{ MHz}$	$C_{os}$	typ.	3,5	pF
	Noise figure at optimum source admittance				
→	$G_S = 0,95 \text{ mS}$ ; $-B_S = 5,0 \text{ mS}$ ; $f = 100 \text{ MHz}$	F	typ.	1,9	dB
→	$G_S = 1,20 \text{ mS}$ ; $-B_S = 5,7 \text{ mS}$ ; $f = 200 \text{ MHz}$	F	typ.	2,3	dB
			<	3,0	dB
	Cross modulation at $f = 200 \text{ MHz}$				
	Wanted signal at $f_o = 197,5 \text{ MHz}$				
	Unwanted signal at $f_{int} = 202,5 \text{ MHz}$				
	Interference voltage at $g_1$ for $K = 1\%$	$V_{int}$	typ.	100	mV <sup>1)</sup>

1) Cross modulation is defined here as the voltage at  $g_1$  of an unwanted signal with 80% modulation depth, giving 0,8% modulation depth on the wanted signal (a. m. definition).





circles of constant noise figure

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as line current interruptor in telephone sets and for application in relay, high-speed and line-transformer drivers.

### Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

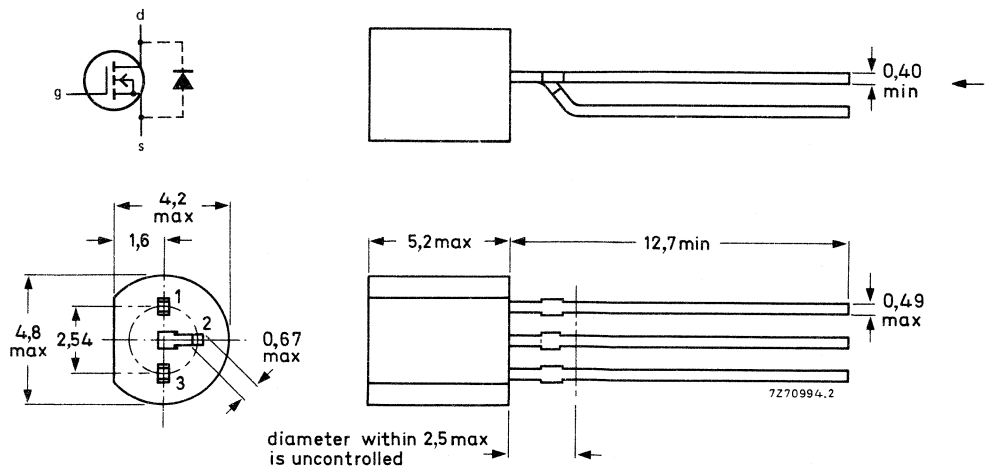
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage	$V_{GS}$	max.	15 V
Drain current (d.c.)	$I_D$	max.	120 mA
Total power dissipation up to $T_C = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	500 mW
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$
Drain-source ON-resistance $V_{GS} = 2,6\text{ V}; I_D = 20\text{ mA}$	$R_{DSon}$	max.	28 $\Omega$

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DSS}$	max.	200 V
Drain-gate voltage	$V_{DGS}$	max.	200 V
Gate-source voltage	$V_{GS}$	max.	15 V
Drain current (d.c.)	$I_D$	max.	120 mA
Total power dissipation up to $T_C = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	500 mW
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient	$R_{th\ j-a}$	=	150 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0; I_D = 100\ \mu\text{A}$	$V_{(BR)DS}$	>	200 V
Gate-source leakage current $V_{GS} = 15\text{ V}; V_{DS} = 0$	$I_{Gsoff}$	<	10 nA
Drain cut-off current $V_{DS} = 130\text{ V}; V_{GS} = 0$	$I_{DSS}$	<	30 nA
$V_{DS} = 70\text{ V}; V_{GS} = 0,2\text{ V}$	$I_{DSX}$	<	1 $\mu\text{A}$
Drain-source ON-resistance $V_{GS} = 2,6\text{ V}; I_D = 20\text{ mA}$	$r_{DSon}$	typ. <	15 $\Omega$ 28 $\Omega$



## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

### Features:

- Very low  $R_{DSon}$ .
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

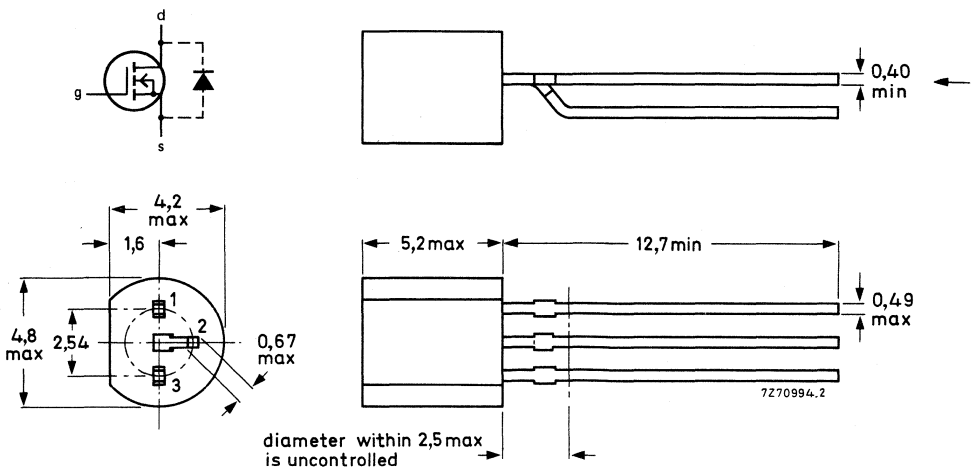
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	60 V	
Gate-source voltage	$V_{GS}$	max.	15 V	
Drain current (d.c.)	$I_D$	max.	500 mA	
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	830 mW	←
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$	
Drain-source ON-resistance $V_{GS} = 10\text{ V}; I_D = 200\text{ mA}$	$R_{DSon}$	max.	5 $\Omega$	

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	60 V
Drain-gate voltage	$V_{DG}$	max.	60 V
Gate-source voltage	$V_{GS}$	max.	15 V
→ Drain current (d.c.) at $T_c = 25\text{ }^\circ\text{C}$	$I_D$	max.	500 mA
→ Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	830 mW
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient	$R_{th\ j-a}$	=	150 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

→ Drain-source breakdown voltage $V_{GS} = 0; I_D = 100\text{ }\mu\text{A}$	$V_{(BR)DS}$	> typ.	60 V 90 V
Gate threshold voltage $V_{GS} = V_{DS}; I_D = 1\text{ mA}$	$V_{GS(th)}$	> <	0,8 V 3,0 V
Gate-source leakage current $V_{GS} = 15\text{ V}; V_{DS} = 0$	$I_{GSoff}$	<	10 nA
Drain cut-off current $V_{DS} = 25\text{ V}; V_{GS} = 0$	$I_{DSS}$	<	0,5 $\mu\text{A}$
Drain-source ON-resistance * $V_{GS} = 10\text{ V}; I_D = 200\text{ mA}$	$r_{DSon}$	typ. <	3,5 $\Omega$ 5,0 $\Omega$
→ Forward transconductance * $V_{DS} = 10\text{ V}; I_D = 200\text{ mA};$ $f = 1\text{ kHz}$	$g_{fs}$	typ.	200 mS
→ Capacitances at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{iss}$	typ.	25 pF
	$C_{os}$	typ.	22 pF
	$C_{rs}$	typ.	6 pF
Switching times at $I_D = 200\text{ mA}$ $I_D = 200\text{ mA}; V_{DS} = 50\text{ V};$	$t_{on}$	typ. <	4 ns 10 ns
→ $V_{GS} = 0\text{ to }10\text{ V}$	$t_{off}$	typ. <	4 ns 10 ns

\*  $t_p = 80\text{ }\mu\text{s}; \delta = 0,01.$

## MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel depletion mode type. The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

### Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

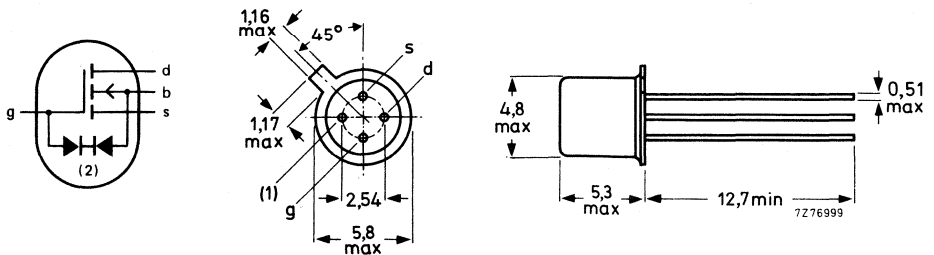
### QUICK REFERENCE DATA

		BSD10	BSD12
Drain-source voltage	$V_{DS}$ max.	10	20 V
Gate-source voltage	$V_{GS}$ max.	+10 -30	+20 V -40 V
Drain current (d.c.)	$I_D$ max.	50 mA	
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (free air)	$P_{tot}$ max.	275 mW	
Junction temperature	$T_j$ max.	125 $^\circ\text{C}$	
Drain-source ON-resistance $V_{GS} = 10\text{ V}; V_{SB} = 0; I_D = 1\text{ mA}$	$R_{DSon}$ <	30 $\Omega$	
Feedback capacitance $V_{GS} = V_{BS} = -5\text{ V};$ $V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	$C_{rss}$ typ.	0,6	pF

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) Substrate (b) connected to case.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			<u>BSD10</u>	<u>BSD12</u>
Drain-source voltage	$V_{DS}$	max.	10	20 V
Source-drain voltage	$V_{SD}$	max.	10	20 V
Drain-substrate voltage	$V_{DB}$	max.	15	25 V
Source-substrate voltage	$V_{SB}$	max.	15	25 V
Gate-substrate voltage	$V_{GB}$	max.	+15 -15	+15 V -15 V
Gate-source voltage	$V_{GS}$	max.	+15 -30	+15 V -40 V
Drain current (d.c.)	$I_D$	max.	50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ in free air	$P_{tot}$	max.	275	mW
Storage temperature	$T_{stg}$		-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	125	$^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient	$R_{th\ j-a}$	=	360	K/W
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**CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

			<u>BSD10</u>	<u>BSD12</u>
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5\text{ V}; I_S = 10\text{ nA}$	$V_{(BR)DSX}$	>	10	20 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$	$V_{(BR)SDX}$	>	10	20 V
Drain-substrate breakdown voltage $V_{GB} = 0; I_D = 10\text{ nA};$ open source	$V_{(BR)DBO}$	>	15	25 V
Source-substrate breakdown voltage $V_{GB} = 0; I_S = 10\text{ nA};$ open drain	$V_{(BR)SBO}$	>	15	25 V
Drain-source leakage current $V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 10\text{ V}$	$I_{DSoff}$	typ.	1,0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5\text{ V}; V_{SD} = 10\text{ V}$	$I_{SDoff}$	typ.	1,0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0; V_{GB} = \pm 15\text{ V}$	$I_{GSoff}$	<	10	nA
Forward transconductance at $f = 1\text{ kHz}$ $V_{DS} = 10\text{ V}; V_{SB} = 0; I_S = 20\text{ mA}$	$g_{fs}$	> typ.	10 15	mS mS

Gate-source cut-off voltage

$V_{DS} = 10 \text{ V}; V_{SB} = 0;$   
 $I_S = 10 \mu\text{A}$

$-V_{(P)GS} < 2,0 \text{ V}$

Drain-source ON-resistance

$I_D = 1 \text{ mA}; V_{SB} = 0$   
 $V_{GS} = 5 \text{ V}$

$r_{DSon}$	typ.	25 $\Omega$
	<	50 $\Omega$
$r_{DSon}$	typ.	15 $\Omega$
	<	30 $\Omega$

$V_{GS} = 10 \text{ V}$

Capacitances at  $f = 1 \text{ MHz}$  (see Fig. 2)

$V_{GS} = V_{BS} = -5 \text{ V}; V_{DS} = 10 \text{ V}$

Feed-back capacitance

$C_{rss}$  typ. 0,6 pF

Input capacitance

$C_{iss}$  typ. 2,3 pF

Output capacitance

$C_{oss}$  typ. 1,9 pF

Switching times (see Fig. 3)

$V_{DD} = 10 \text{ V}; V_i = -5 \text{ to } 0 \text{ V}$

$t_{on}$  typ. 1,0 ns  
 $t_{off}$  typ. 5,0 ns

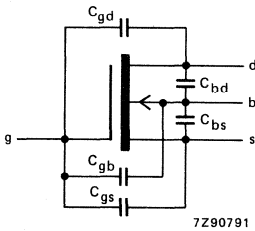


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$

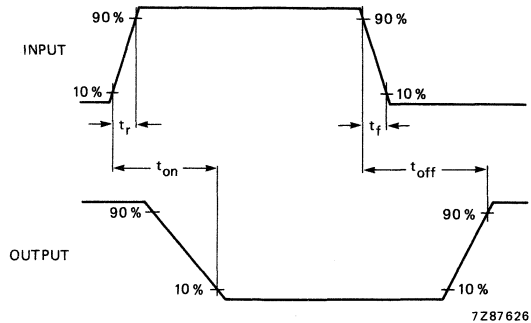
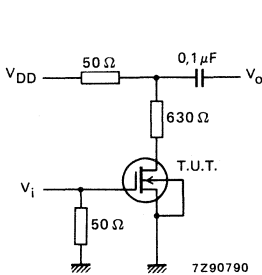


Fig. 3 Switching times and input and output waveforms;

$R_i = 50 \Omega; t_r < 0,5 \text{ ns}; t_f < 1,0 \text{ ns}; t_p = 20 \text{ ns}; \delta < 0,01.$



## MOSFET N-CANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistors of the N-channel depletion mode type. The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

### Applications:

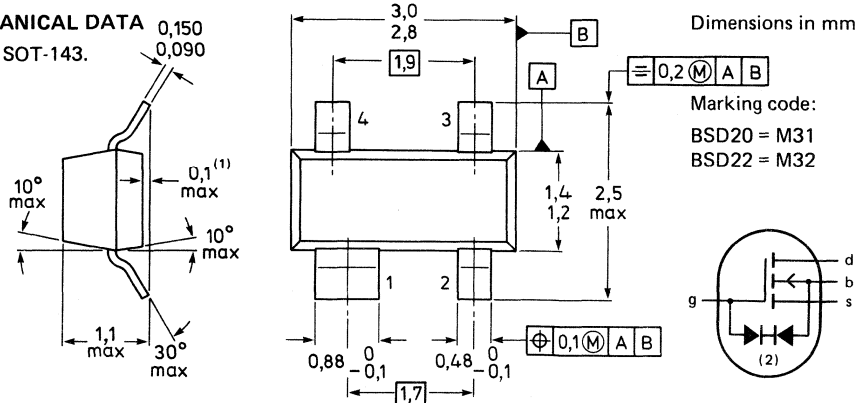
- analog and/or digital switch
- switch driver
- convertor
- chopper

### QUICK REFERENCE DATA

		BSD20	BSD22
Drain-source voltage	$V_{DS}$	max. 10	20 V
Gate-source voltage	$V_{GS}$	max. +10 -30	+20 V -40 V
Drain current (d.c.)	$I_D$	max. 50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max. 230	mW
Junction temperature	$T_j$	max. 125	$^\circ\text{C}$
Drain-source ON-resistance $V_{GS} = 10\text{ V}; V_{SB} = 0; I_D = 1\text{ mA}$	$R_{DSon}$	< 30	$\Omega$
Feed-back capacitance $V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	$C_{rss}$	typ. 0,6	pF

### MECHANICAL DATA

Fig. 1 SOT-143.



(1) Also available in 0,1 – 0,2 mm version. TOP VIEW

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		BSD20		BSD22	
Drain-source voltage	$V_{DS}$	max.	10	20	V
Source-drain voltage	$V_{SD}$	max.	10	20	V
Drain-substrate voltage	$V_{DB}$	max.	15	25	V
Source-substrate voltage	$V_{SB}$	max.	15	25	V
Gate-substrate voltage	$V_{GB}$	max.	$\pm 15$	$\pm 25$	V
Gate-source voltage	$V_{GS}$	max.	+15 -30	+15 -40	V
Drain current (d.c.)	$I_D$	max.		50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ *	$P_{tot}$	max.		230	mW
Storage temperature	$T_{stg}$			-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.		125	$^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient in free air *	$R_{th\ j-a}$	=	430	K/W
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**CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

		BSD20		BSD22	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5\text{ V}; I_S = 10\text{ nA}$	$V_{(BR)DSX}$	>	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$	$V_{(BR)SDX}$	>	10	20	V
Drain-substrate breakdown voltage $V_{GB} = 0; I_D = 10\text{ nA};$ open source	$V_{(BR)DBO}$	>	15	25	V
Source-substrate breakdown voltage $V_{GB} = 0; I_S = 10\text{ nA};$ open drain	$V_{(BR)SBO}$	>	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 20\text{ V}$	$I_{DSoff}$	typ.		1,0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5\text{ V}; V_{SD} = 20\text{ V}$	$I_{SDoff}$	typ.		1,0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0; V_{GB} = \pm 15\text{ V}$	$I_{GSoff}$	<		10	nA

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,8 mm.



Forward transconductance at  $f = 1 \text{ kHz}$

$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 20 \text{ mA}$

$g_{fs}$	>	10 mS
	typ.	15 mS

Gate-source cut-off voltage

$V_{DS} = 10 \text{ V}; V_{SB} = 0;$

$I_S = 10 \mu\text{A}$

$-V_{(P)GS}$	<	2,0 V
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Drain-source ON-resistance

$I_D = 1 \text{ mA}; V_{SB} = 0;$

$V_{GS} = 5 \text{ V}$

$r_{DSon}$	typ.	25 $\Omega$
	<	50 $\Omega$

$V_{GS} = 10 \text{ V}$

$r_{DSon}$	typ.	15 $\Omega$
	<	30 $\Omega$

Capacitances at  $f = 1 \text{ MHz}$

$V_{GS} = V_{BS} = -10 \text{ V}; V_{DS} = 10 \text{ V}$

Feed-back capacitance

$C_{rss}$	typ.	0,6 pF
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Input capacitance

$C_{iss}$	typ.	1,5 pF
-----------	------	--------

Output capacitance

$C_{oss}$	typ.	1,0 pF
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Switching times (see Fig. 2)

$V_{DD} = 10 \text{ V}; V_i = 5 \text{ V}$

$t_{on}$	typ.	1,0 ns
$t_{off}$	typ.	5,0 ns

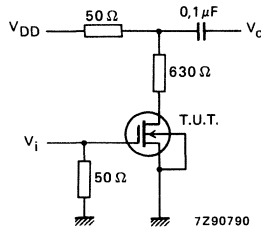


Fig. 2 Switching times test circuit.



## MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type. These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

### Applications:

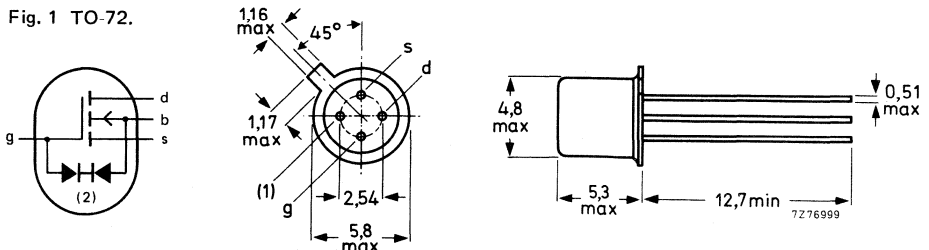
- analogue and/or digital switch
- switch driver
- converters
- choppers

### QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	$V_{DS}$	max.	10	10	20	20	V
Gate-source voltage	$V_{GS}$	max.	$\pm 40$	+ 15 - 30	$\pm 40$	+ 15 - 40	V
Drain current (d.c.)	$I_D$	max.	50				mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (free air)	$P_{tot}$	max.	275				mW
Drain-source resistance $I_D = 1\text{ mA}; V_{SB} = 0; V_{GS} = 15\text{ V}$	$r_{DSon}$	typ.	25				$\Omega$
Feedback capacitance $V_{GS} = V_{BS} = -15\text{ V};$ $V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	$C_{rss}$	typ.	0,6				pF
Junction temperature	$T_j$	max.	125				$^\circ\text{C}$

### MECHANICAL DATA

Fig. 1 TO-72.



(1) Substrate (b) connected to case.

(2) Diode protection on types BSD213 and BSD215 only.

# BSD212 to BSD215

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	$V_{DS}$	max.	10	10	20	20	V
Source-drain voltage	$V_{SD}$	max.	10	10	20	20	V
Drain-substrate voltage	$V_{DB}$	max.	15	15	25	25	V
Source-substrate voltage	$V_{SB}$	max.	15	15	25	25	V
Gate-substrate voltage	$V_{GB}$	max.	$\pm 40$	$\pm 15$	$\pm 40$	$\pm 15$	V
Gate-source voltage	$V_{GS}$	max.	$\pm 40$	+15 -30	$\pm 40$	+15 -40	V
Gate-drain voltage	$V_{GD}$	max.	$\pm 40$	+15 -30	$\pm 40$	+15 -40	V
Drain current (d.c.)	$I_D$	max.	50				mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (free air)	$P_{tot}$	max.	275				mW
Storage temperature	$T_{stg}$		-65 to +175				$^\circ\text{C}$
Junction temperature	$T_j$	max.	125				$^\circ\text{C}$

## THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	360				K/W
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## CHARACTERISTICS

$T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5\text{ V}$ ; $I_S = 10\text{ nA}$	$V_{(BR)DSX} >$		10	10	20	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5\text{ V}$ ; $I_D = 10\text{ nA}$	$V_{(BR)SDX} >$		10	10	20	20	V
Drain-substrate breakdown voltage $V_{GB} = 0$ ; $I_D = 10\text{ nA}$ ; open source	$V_{(BR)DBO} >$		15	15	25	25	V
Source-substrate breakdown voltage $V_{GB} = 0$ ; $I_S = 10\text{ nA}$ ; open drain	$V_{(BR)SBO} >$		15	15	25	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5\text{ V}$ ; $V_{DS} = 10\text{ V}$	$I_{DSoff}$	typ.	1,0	1,0	—	—	nA
$V_{GS} = V_{BS} = -5\text{ V}$ ; $V_{DS} = 20\text{ V}$	$I_{DSoff}$	typ.	—	—	1,0	1,0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5\text{ V}$ ; $V_{SD} = 10\text{ V}$	$I_{SDoff}$	typ.	1,0	1,0	—	—	nA
$V_{GD} = V_{BD} = -5\text{ V}$ ; $V_{SD} = 20\text{ V}$	$I_{SDoff}$	typ.	—	—	1,0	1,0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$ ; $V_{GB} = \pm 40\text{ V}$	$I_{GBS}$	$<$	0,1	—	0,1	—	nA
$V_{DB} = V_{SB} = 0$ ; $V_{GB} = \pm 15\text{ V}$	$I_{GBS}$	$<$	—	10	—	10	nA
Threshold voltage $V_{DS} = V_{GS} = V_{GS(th)}$ $V_{SB} = 0$ ; $I_S = 1\text{ }\mu\text{A}$	$V_{GS(th)}$		0,1 to 2,0				V

		BSD212	BSD213	BSD214	BSD215	
Drain-source resistance						
$I_D = 1,0 \text{ mA}; V_{SB} = 0;$						
$V_{GS} = 5 \text{ V}$	$r_{DSon}$ typ.	50	50	50	50	$\Omega$
	<	70	70	70	70	$\Omega$
$V_{GS} = 10 \text{ V}$	$r_{DSon}$ typ.	30	30	30	30	$\Omega$
	<	45	45	45	45	$\Omega$
$V_{GS} = 15 \text{ V}$	$r_{DSon}$ typ.	25	25	25	25	$\Omega$
$V_{GS} = 25 \text{ V}$	$r_{DSon}$ typ.	15		15		$\Omega$

**DYNAMIC CHARACTERISTICS**

Forward transconductance at  $f = 1 \text{ kHz}$

$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 20 \text{ mA}$	$g_{fs}$ typ.	15	
	>	10	mS

Capacitance at  $f = 1 \text{ MHz}$  (see Fig. 2)

$V_{GS} = V_{BS} = -15 \text{ V}; V_{DS} = 10 \text{ V}$			
Feed-back capacitance	$C_{rss}$ typ.	0,6	pF
Input capacitance	$C_{iss}$ typ.	2,3	pF
Output capacitance	$C_{oss}$ typ.	1,9	pF

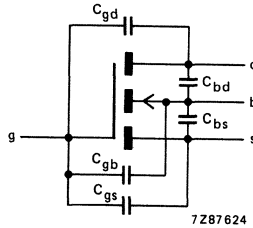


Fig. 2 Capacitances model.

$$C_{iss} = C_{GS} + C_{GD} + C_{GB}$$

$$C_{oss} = C_{GD} + C_{BD}$$

$$C_{rss} = C_{GD}$$

DYNAMIC CHARACTERISTICS (continued)

Switching times (see Fig. 3)

$V_{DD} = 10\text{ V}; V_i = 5\text{ V}$

$t_{on}$	typ.	1,0	ns
$t_{off}$	typ.	5,0	ns

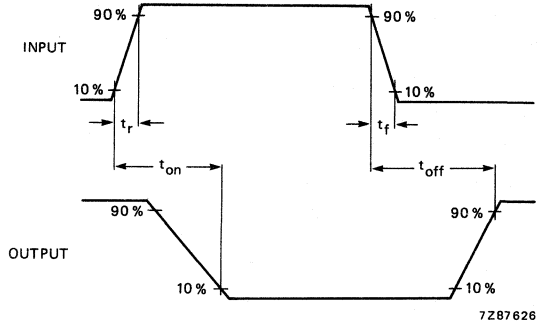
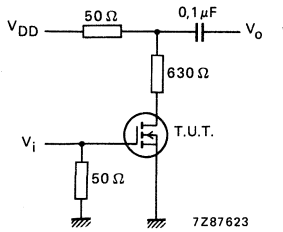


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

$R_i = 50\ \Omega$

$t_r < 0,5\text{ ns}$

$t_f < 1,0\text{ ns}$

$t_p = 20\text{ ns}$

$\delta < 0,01$

## MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver

### QUICK REFERENCE DATA

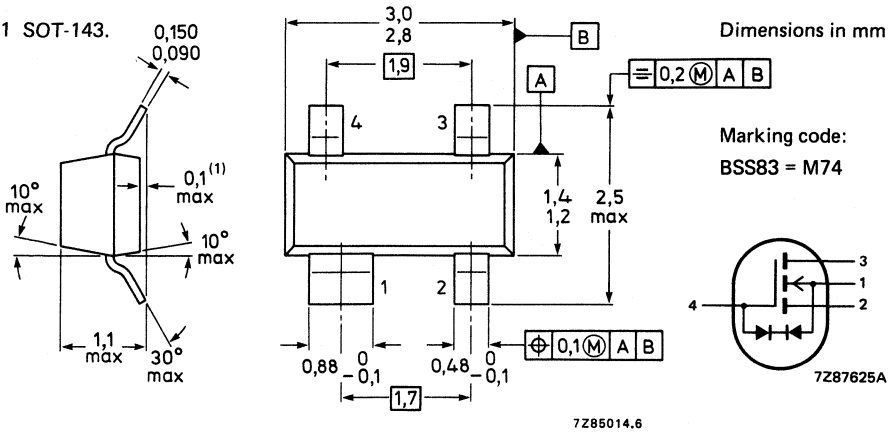
Drain-source voltage	$V_{DS}$	max.	10 V
Source-drain voltage	$V_{SD}$	max.	10 V
Drain-substrate voltage	$V_{DB}$	max.	15 V
Source-substrate voltage	$V_{SB}$	max.	15 V
Drain current (d.c.)	$I_D$	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	230 mW
Gate-source cut-off voltage			
$V_{DS} = V_{GS}; V_{SB} = 0;$	$V_{(P)GS}$	>	0,1 V
$I_D = 1\text{ }\mu\text{A}$		<	2,0 V
Drain-source ON-resistance			
$V_{GS} = 10\text{ V}; V_{SB} = 0; I_D = 0,1\text{ mA}$	$r_{DSon}$	<	45 $\Omega$
Feed-back capacitance			
$V_{GS} = V_{BS} = -15\text{ V};$			
$V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	$C_{rss}$	typ.	0,6 pF

### MECHANICAL DATA

SOT-143 (see Fig. 1).

See also *Soldering recommendations*.

Fig. 1 SOT-143.



(1) Also available in 0,1 – 0,2 mm version. TOP VIEW

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	10 V
Source-drain voltage	$V_{SD}$	max.	10 V
Drain-substrate voltage	$V_{DB}$	max.	15 V
Source-substrate voltage	$V_{SB}$	max.	15 V
Drain current (d.c.)	$I_D$	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}^*$	$P_{tot}$	max.	230 mW*
Storage temperature	$T_{stg}$		-65 to +150 °C
Junction temperature	$T_j$	max.	125 °C

**THERMAL RESISTANCE**

From junction to ambient in free air*	$R_{th\ j-a}$	=	430 K/W*
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**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5\text{ V}; I_D = 10\text{ nA}$	$V_{(BR)DSX}$	>	10 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$	$V_{(BR)SDX}$	>	10 V
Drain-substrate breakdown voltage $V_{CB} = 0; I_D = 10\text{ nA};$ open source	$V_{(BR)DBO}$	>	15 V
Source-substrate breakdown voltage $V_{CB} = 0; I_D = 10\text{ nA};$ open drain	$V_{(BR)SBO}$	>	15 V
Drain-source leakage current $V_{GS} = V_{BS} = -2\text{ V}; V_{DS} = 6,6\text{ V}$	$I_{DSoff}$	<	10 nA

\* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.



Source-drain leakage current

$V_{GD} = V_{BD} = -2 \text{ V}; V_{SD} = 6,6 \text{ V}$

$I_{SDoff} < 10 \text{ mA}$

Forward transconductance at  $f = 1 \text{ kHz}$

$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 20 \text{ mA}$

$g_{fs} > 10 \text{ mS}$   
typ. 15 mS

Gate-source cut-off voltage

$V_{DS} = V_{GS}; V_{SB} = 0; I_D = 1 \mu\text{A}$

$V_{(P)GS} > 0,1 \text{ V}$   
< 2,0 V

Drain-source ON-resistance

$I_D = 0,1 \text{ mA};$

$V_{GS} = 5 \text{ V}; V_{SB} = 0$

$r_{DSon} < 70 \Omega$

$V_{GS} = 10 \text{ V}; V_{SB} = 0$

$r_{DSon} < 45 \Omega$

$V_{GS} = 3,2 \text{ V}; V_{SB} = 6,8 \text{ V (see Fig. 4)}$

typ. 80  $\Omega$   
< 120  $\Omega$  ←

Gate-substrate zener voltages

$V_{DB} = V_{SB} = 0; -I_C = 10 \mu\text{A}$

$V_{Z(1)} > 12,5 \text{ V}$

$V_{DB} = V_{SB} = 0; +I_G = 10 \mu\text{A}$

$V_{Z(2)} > 12,5 \text{ V}$

Capacitances at  $f = 1 \text{ MHz}$

$V_{GS} = V_{BS} = -15 \text{ V}; V_{DS} = 10 \text{ V}$

Feed-back capacitance

$C_{rss}$  typ. 0,6 pF

Input capacitance

$C_{iss}$  typ. 1,5 pF

Output capacitance

$C_{oss}$  typ. 1,0 pF

Switching times (see Fig. 2)

$V_{DD} = 10 \text{ V}; V_i = 5 \text{ V}$

$t_{on}$  typ. 1,0 ns

$t_{off}$  typ. 5,0 ns

Pulse generator:

$R_i = 50 \Omega$

$t_r < 0,5 \text{ ns}$

$t_f < 1,0 \text{ ns}$

$t_p = 20 \text{ ns}$

$\delta < 0,01$

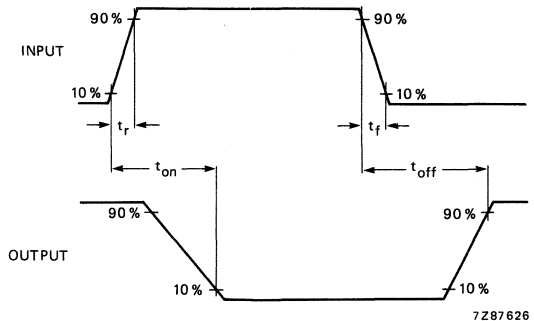
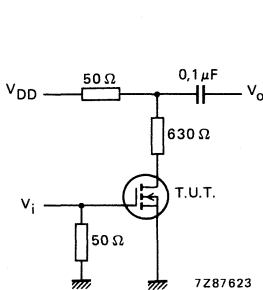


Fig. 2 Switching times test circuit and input and output waveforms.



## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

**Features:**

- Very low  $R_{DSon}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

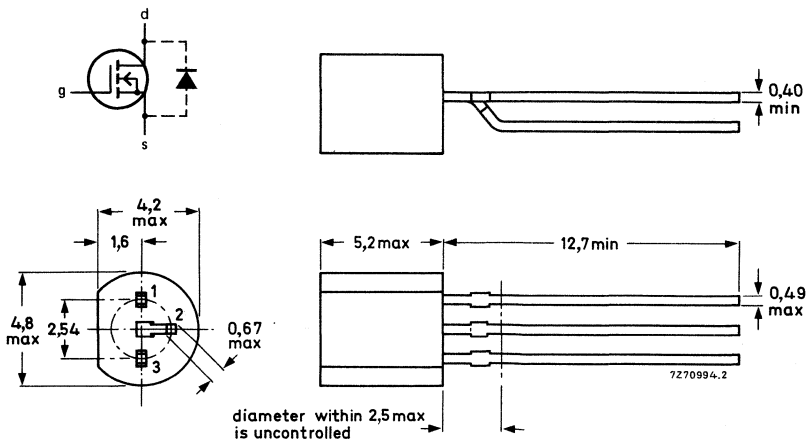
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GS}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. max.	2 $\Omega$ 4 $\Omega$
Transfer admittance $I_D = 500\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	300 mS

**MECHANICAL DATA**

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,5 A
Drain current (peak)	$I_{DM}$	max.	1,0 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient*	$R_{th\ j-a}$		125 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	>	80 V
Drain-source leakage current $V_{DS} = 60\text{ V}; V_{GS} = 0$	$I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance (see Fig. 4) $I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	2,0 $\Omega$ 4,0 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 500\text{ mA}; V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	300 mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{is}$	typ.	45 pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{os}$	typ.	30 pF
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	8 pF
Switching times (see Figs 2 and 3) $I_D = 500\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$ $t_{off}$	< <	10 ns 15 ns

\* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

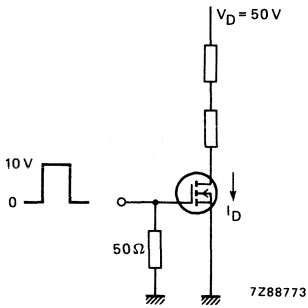


Fig. 2 Switching times test circuit.

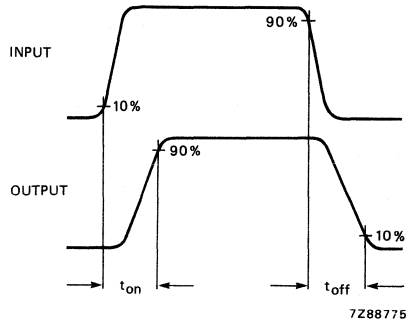


Fig. 3 Input and output waveforms.

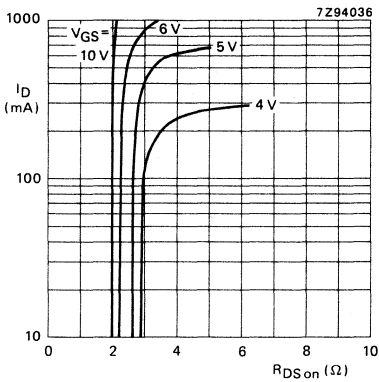


Fig. 4  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

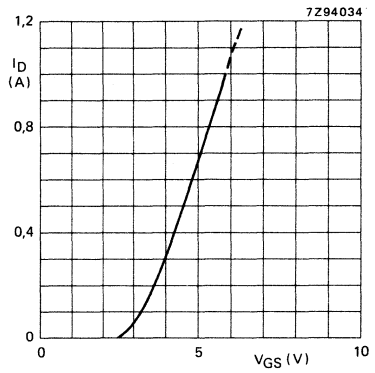


Fig. 5  $T_j = 25\text{ }^\circ\text{C}$ ; typical values at  $V_{DS} = 10\text{ V}$ .

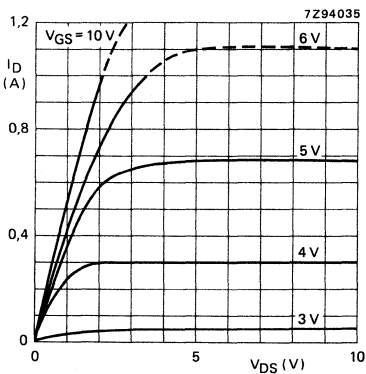


Fig. 6  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

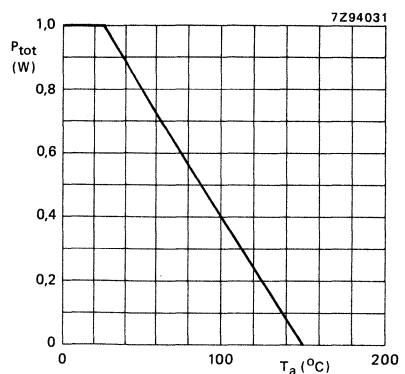


Fig. 7 Power derating curve.

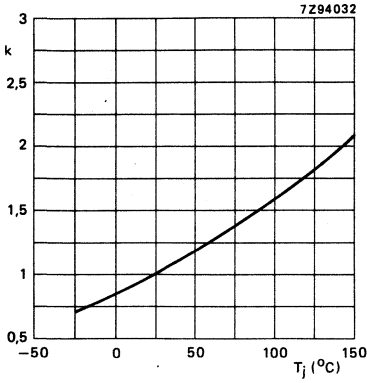


Fig. 8  $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$ ; typ. values at 500 mA/10 V.

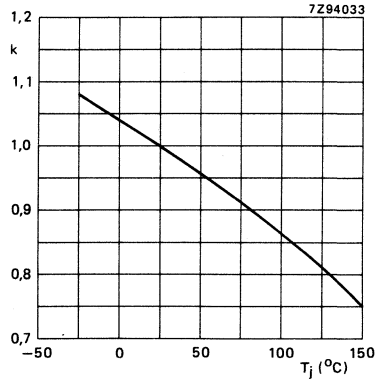


Fig. 9  $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$ ;  $V_{GS(th)}$  at 1 mA; typical values.

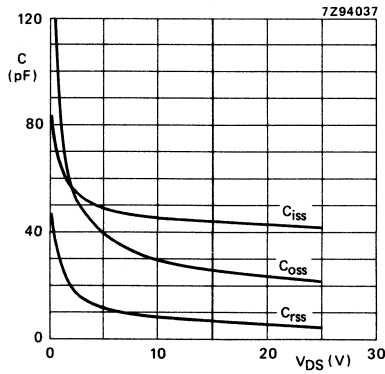


Fig. 10  $T_j = 25\ ^\circ C$ ;  $V_{GS} = 0$ ;  $f = 1\ MHz$ ; typical values.

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

**Features:**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

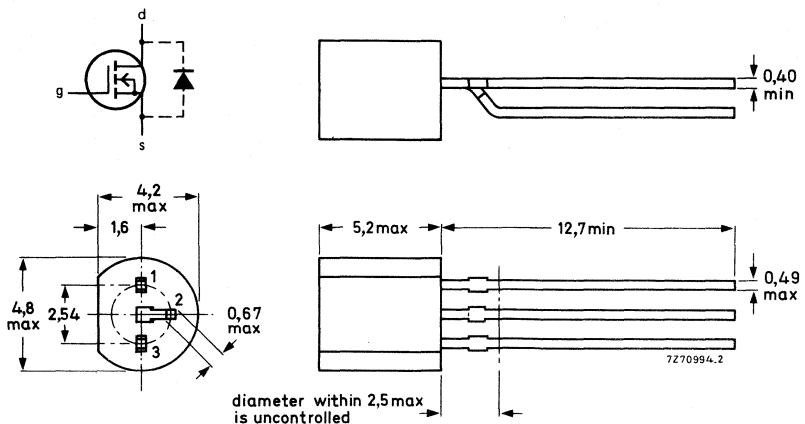
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Total power dissipation up to $T_{amb} = 25$ °C	$P_{tot}$	max.	0,83 W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DSon}$	typ. max.	7 $\Omega$ 10 $\Omega$
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V; $f = 1$ kHz	$ y_{fs} $	typ.	150 mS

**MECHANICAL DATA**

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Drain current (peak)	$I_{DM}$	max.	600 mA
Total power dissipation up to $T_{amb} = 25$ °C*	$P_{tot}$	max.	0,83 W
Storage temperature	$T_{stg}$		-65 to + 150 °C
Junction temperature	$T_j$	max.	150 °C

**THERMAL RESISTANCE**

From junction to ambient*	$R_{th\ j-a}$		150 K/W
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**CHARACTERISTICS**

$T_j = 25$  °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ $\mu$ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	80 V
Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$	$I_{DSS}$	<	1,0 $\mu$ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance (see Fig. 4) $I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DSon}$	typ. <	7 $\Omega$ 10 $\Omega$
Transfer admittance at $f = 1$ kHz $I_D = 200$ mA; $V_{DS} = 5$ V	$ y_{fs} $	typ.	150 mS
Input capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{is}$	typ.	15 pF
Output capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{os}$	typ.	13 pF
Feedback capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{rs}$	typ.	3 pF
Switching times (see Figs 2 and 3) $I_D = 200$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	$t_{on}$	typ. <	4 ns 10 ns
	$t_{off}$	typ. <	4 ns 10 ns

\* Transistor mounted on printed circuit board, max. lead length 4 mm.



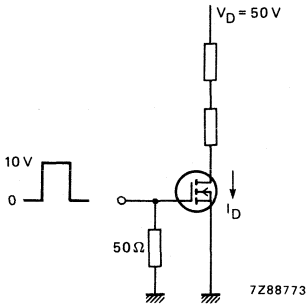


Fig. 2 Switching times test circuit.

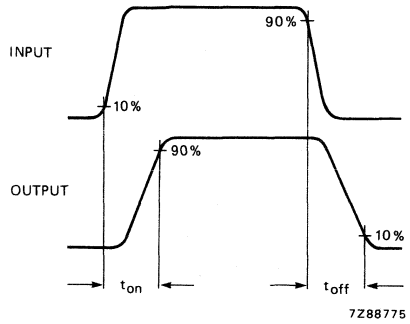


Fig. 3 Input and output waveforms.

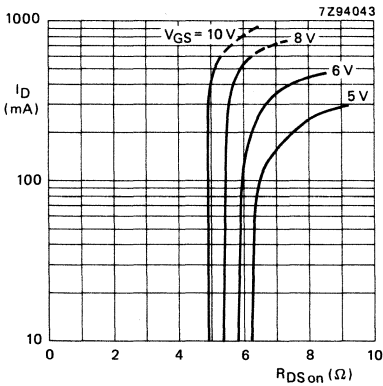


Fig. 4  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

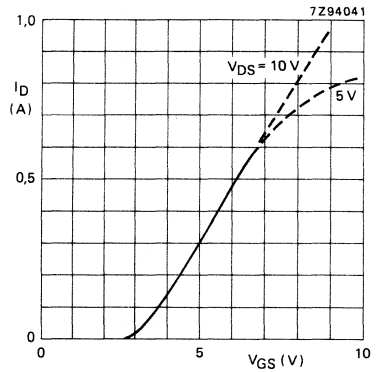


Fig. 5  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

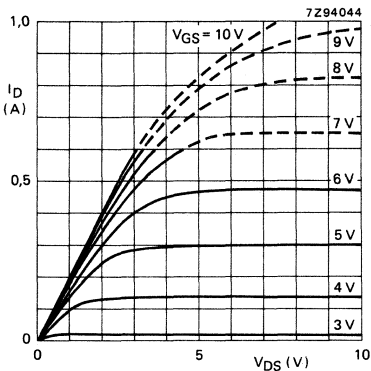


Fig. 6  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

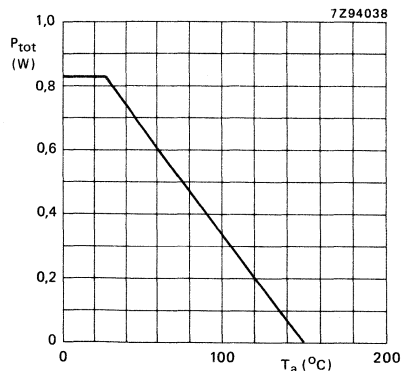


Fig. 7 Power derating curve.

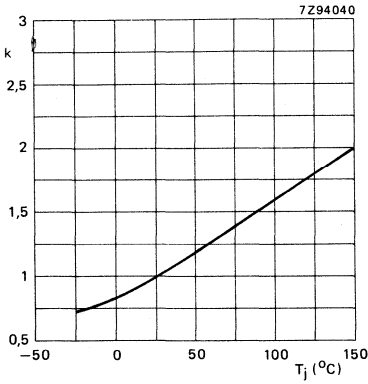


Fig. 8  $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$ ; typ. values at 150 mA/5 V.

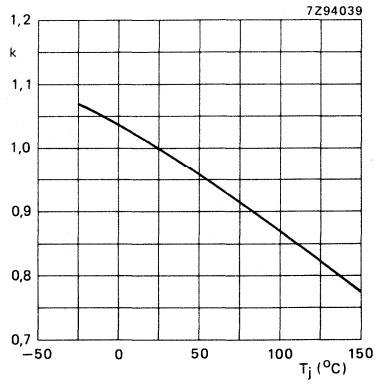


Fig. 9  $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$ ;  $V_{GS(th)}$  at 1 mA; typical values.

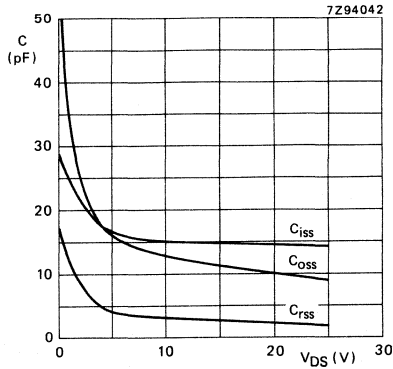


Fig. 10  $T_j = 25\ ^\circ C$ ;  $V_{GS} = 0$ ;  $f = 1\ MHz$ ; typical values.

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

### Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

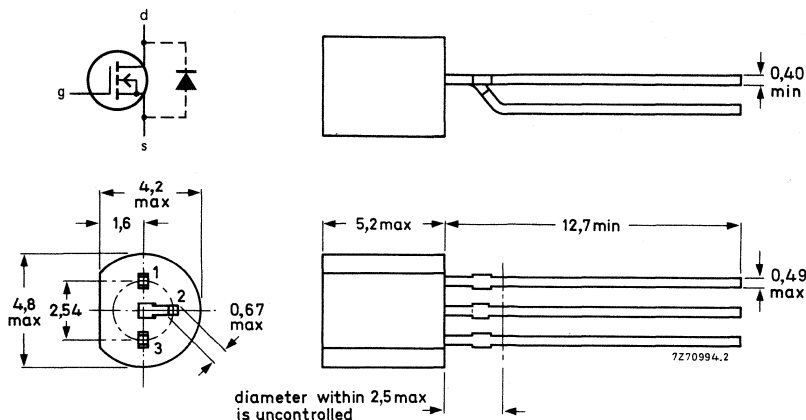
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. max.	6 $\Omega$ 12 $\Omega$
Transfer admittance $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	250 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$V_{GS0}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	250 mA
Drain current (peak)	$I_{DM}$	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient*	$R_{thj-a}$		125 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	>	200 V
Drain-source leakage current $V_{DS} = 160\text{ V}; V_{GS} = 0$	$I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,8 V 2,8 V
Drain-source ON-resistance (see Fig. 4) $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSON}$	typ. <	6 $\Omega$ 12 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	250 mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{is}$	typ.	70 pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{os}$	typ.	20 pF
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	5 pF
Switching times (see Figs 2 and 3) $I_D = 250\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$	typ. <	4 ns 10 ns
	$t_{off}$	typ. <	15 ns 25 ns

\* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

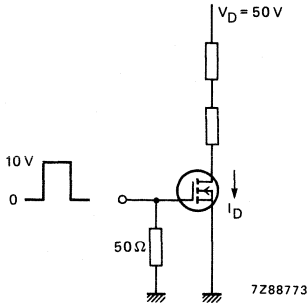


Fig. 2 Switching times test circuit.

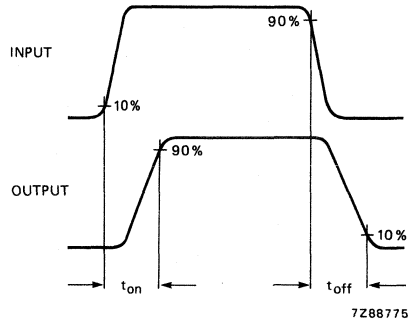


Fig. 3 Input and output waveforms.

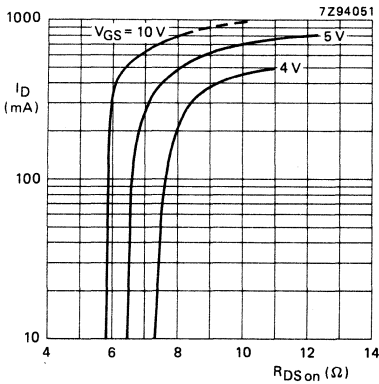


Fig. 4  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

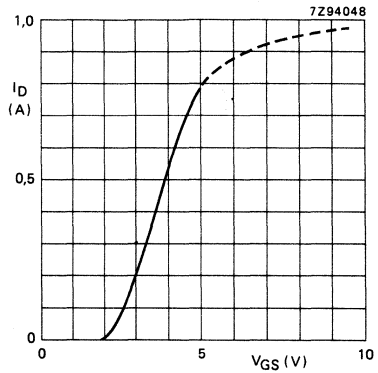


Fig. 5  $T_j = 25\text{ }^\circ\text{C}$ ;  $V_{DS} = 10\text{ V}$ ; typical values.

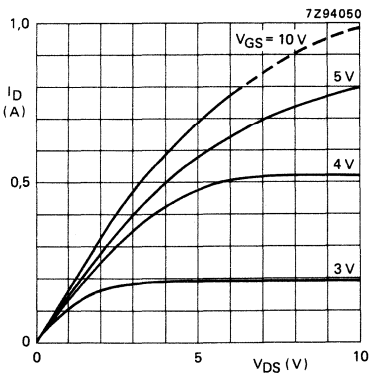


Fig. 6  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

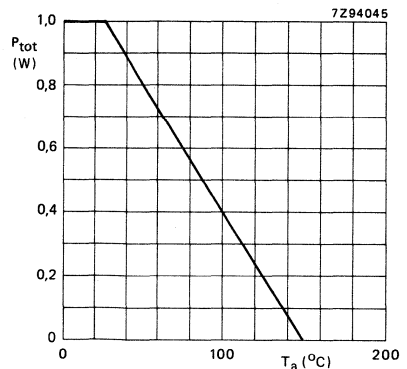


Fig. 7 Power derating curve.

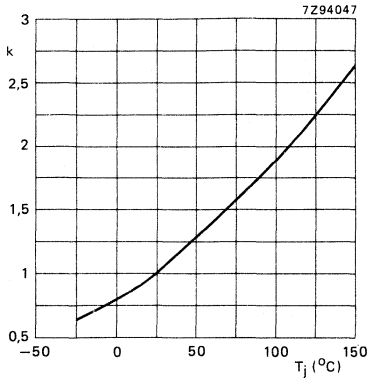


Fig. 8  $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$ ; at 400 mA/10 V; typical values.

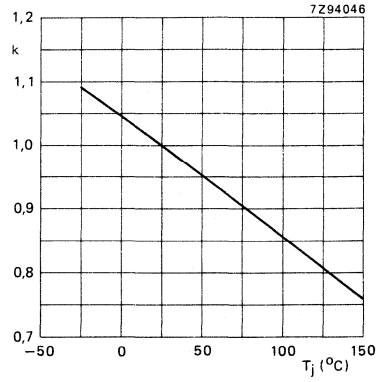


Fig. 9  $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$ ; V<sub>GS(th)</sub> at 1 mA; typical values.

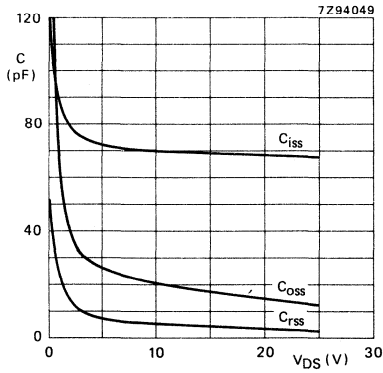


Fig. 10 T<sub>j</sub> = 25 °C; V<sub>GS</sub> = 0; f = 1 MHz; typical values.

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

**Features:**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

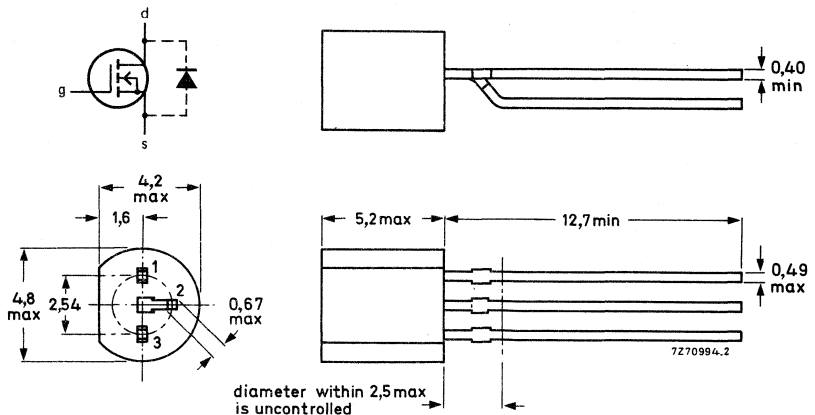
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Total power dissipation up to $T_{amb} = 25^\circ C$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	$R_{DSon}$	typ. max.	7 $\Omega$ 10 $\Omega$
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$ y_{fs} $	typ.	250 mS

**MECHANICAL DATA**

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Drain current (peak)	$I_{DM}$	max.	800 mA
Total power dissipation up to $T_{amb} = 25$ °C*	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-65 to + 150 °C
Junction temperature	$T_j$	max.	150 °C

**THERMAL RESISTANCE**

From junction to ambient*	$R_{tj-a}$		125 K/W
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**CHARACTERISTICS**

$T_j = 25$  °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ $\mu$ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	180 V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	$I_{DSS}$	<	10 $\mu$ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 100$ $\mu$ A; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,7 V 2,7 V
Drain-source ON-resistance (see Fig. 4) $I_D = 15$ mA; $V_{GS} = 3$ V	$R_{DSon}$	typ. <	7 $\Omega$ 10 $\Omega$
$I_D = 300$ mA; $V_{GS} = 10$ V	$R_{DSon}$	typ.	6 $\Omega$
Transfer admittance at $f = 1$ kHz $I_D = 300$ mA; $V_{DS} = 15$ V	$ Y_{fs} $	typ.	250 mS
Input capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{is}$	typ.	50 pF
Output capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{os}$	typ.	20 pF
Feedback capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{rs}$	typ.	6 pF
Switching times (see Figs 2 and 3) $I_D = 300$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	$t_{on}$ $t_{off}$	< <	10 ns 15 ns

\* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.



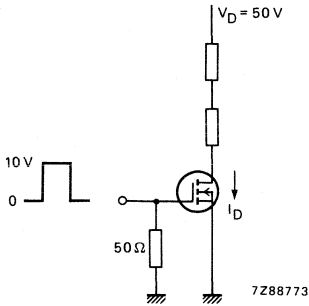


Fig. 2 Switching times test circuit.

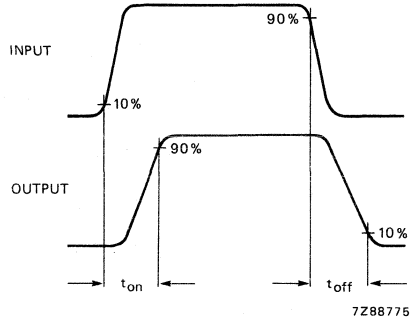


Fig. 3 Input and output waveforms.

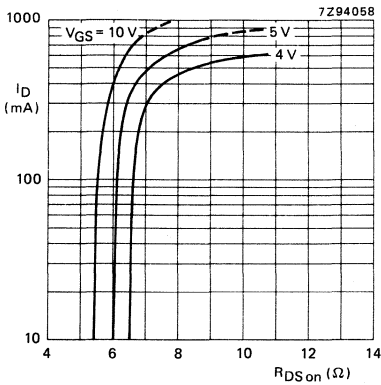


Fig. 4  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

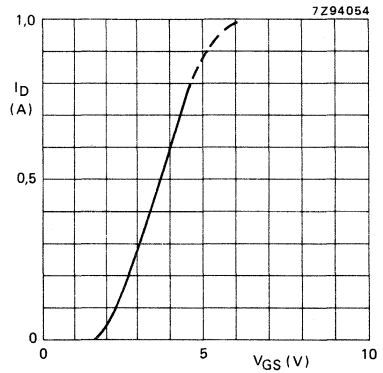


Fig. 5  $T_j = 25\text{ }^\circ\text{C}$ ;  $V_{DS} = 10\text{ V}$ ; typ. values.

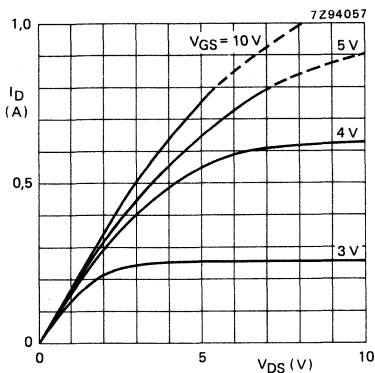


Fig. 6  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

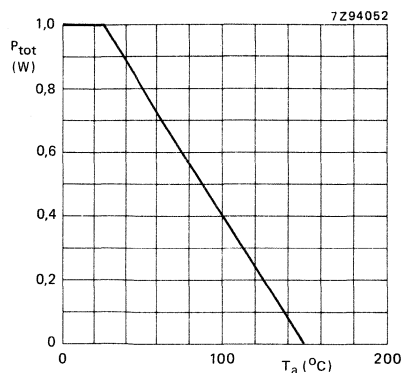


Fig. 7 Power derating curve.

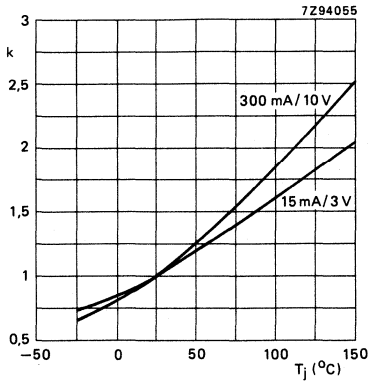


Fig. 8  $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$ ; typical values.

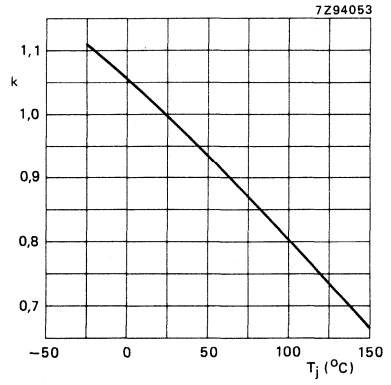


Fig. 9  $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$ ;  $V_{GS(th)}$  at 0,1 mA; typical values.

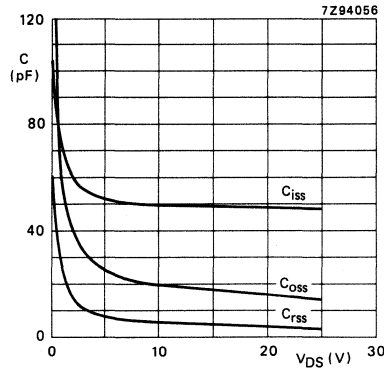


Fig. 10  $T_j = 25\ ^\circ C$ ;  $V_{GS} = 0$ ;  $f = 1\ MHz$ ; typical values.

# HIGH-VOLTAGE N-CHANNEL VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

## QUICK REFERENCE DATA

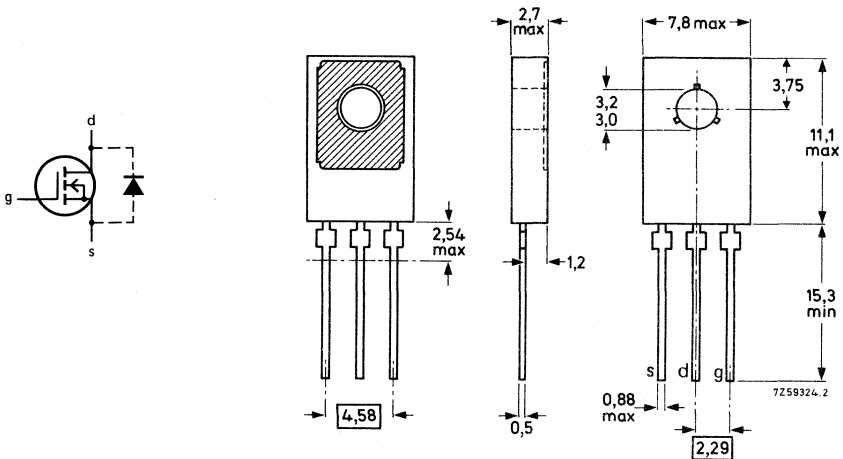
Drain-source voltage	$V_{DS}$	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leq 50 \mu s$ )	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,75 A
Total power dissipation up to $T_{mb} = 75 \text{ }^\circ\text{C}$	$P_{tot}$	max.	15 W
Drain-source ON-resistance $I_D = 500 \text{ mA}; V_{GS} = 10 \text{ V}$	$R_{DSon}$	typ.	15 $\Omega$
Transfer admittance $I_D = 250 \text{ mA}; V_{DS} = 20 \text{ V}; f = 1 \text{ kHz}$	$ y_{fs} $	typ.	400 mS

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leq 50 \mu s$ )	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	$V_{GS0}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,75 A
Drain current (peak)	$I_{DM}$	max.	1,5 A
Total power dissipation up to $T_{mb} = 75 \text{ }^\circ\text{C}$	$P_{tot}$	max.	15 W
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient	$R_{th \text{ j-a}}$	100	K/W
From junction to mounting base	$R_{th \text{ j-mb}}$	5	K/W

**CHARACTERISTICS**

$T_j = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 100 \mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	>	450 V
Drain-source leakage current $V_{DS} = 350 \text{ V}; V_{GS} = 0$	$I_{DSS}$	<	25 $\mu\text{A}$
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate-source cut-off voltage $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$	$V_{(P)GS}$	> <	2,0 V 4,0 V
Drain-source ON-resistance (see Fig. 4) $I_D = 100 \text{ mA}; V_{GS} = 10 \text{ V}$	$R_{DSon}$	typ. <	10 $\Omega$ 14 $\Omega$
$I_D = 500 \text{ mA}; V_{GS} = 10 \text{ V}$	$R_{DSon}$	typ.	15 $\Omega$
Transfer admittance at $f = 1 \text{ kHz}$ $I_D = 250 \text{ mA}; V_{DS} = 20 \text{ V}$	$ y_{fs} $	typ.	400 mS
Input capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 10 \text{ V}; V_{GS} = 0$	$C_{is}$	typ. <	75 pF 100 pF
Output capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 10 \text{ V}; V_{GS} = 0$	$C_{os}$	typ. <	25 pF 35 pF
Feedback capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 10 \text{ V}; V_{GS} = 0$	$C_{rs}$	typ. <	3 pF 5 pF
Switching times (see Figs 2 and 3) $I_D = 100 \text{ mA}; V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ to } 10 \text{ V}$	$t_{on}$	<	10 ns
	$t_{off}$	<	100 ns

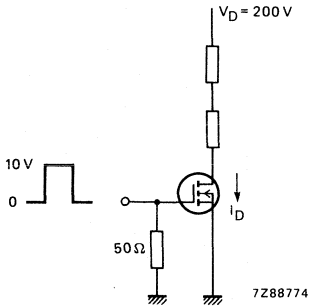


Fig. 2 Switching times test circuit.

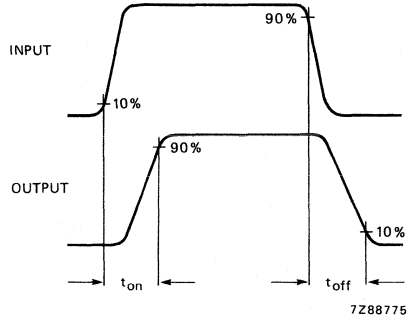


Fig. 3 Input and output waveforms.

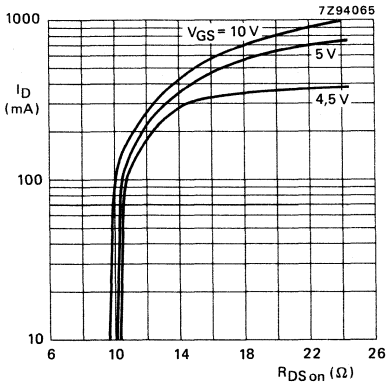


Fig. 4  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

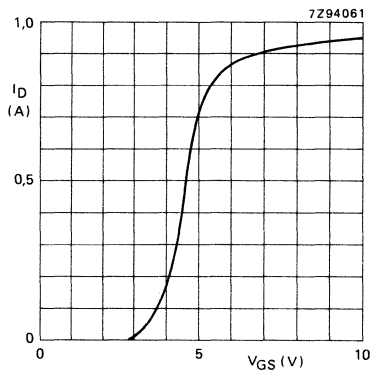


Fig. 5  $T_j = 25\text{ }^\circ\text{C}$ ;  $V_{DS} = 20\text{ V}$ ; typical values.

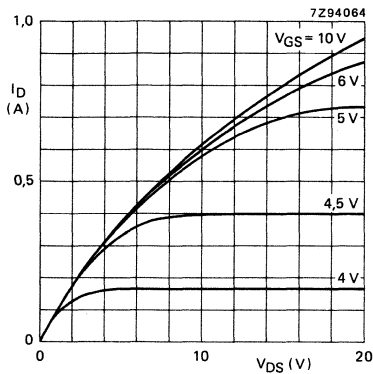


Fig. 6  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

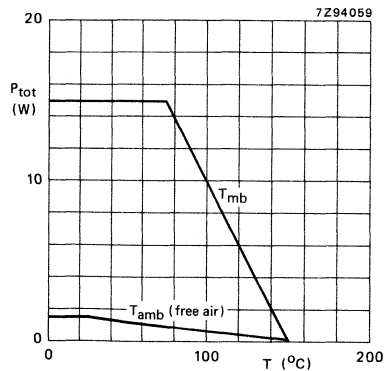


Fig. 7 Power derating curve.

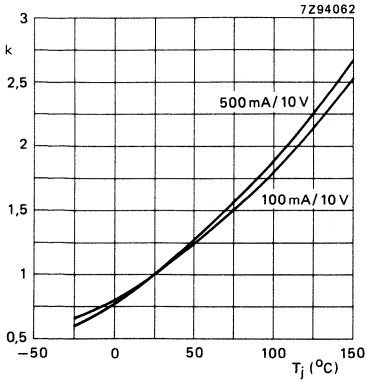


Fig. 8  $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$ ; typical values.

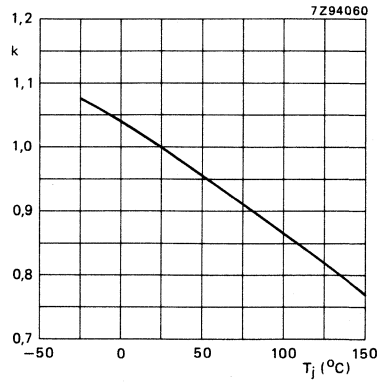


Fig. 9  $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$ ;  $V_{GS(th)}$  at 1 mA; typical values.

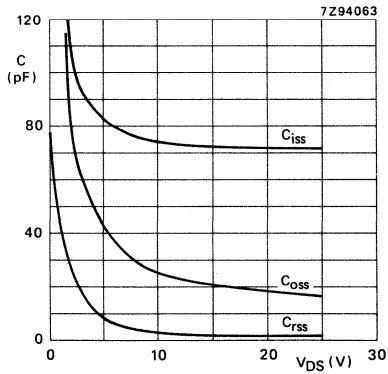


Fig. 10  $T_j = 25\ ^\circ C$ ;  $V_{GS} = 0$ ;  $f = 1\ MHz$ ; typical values.

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

**Features:**

- Very low  $R_{DSon}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

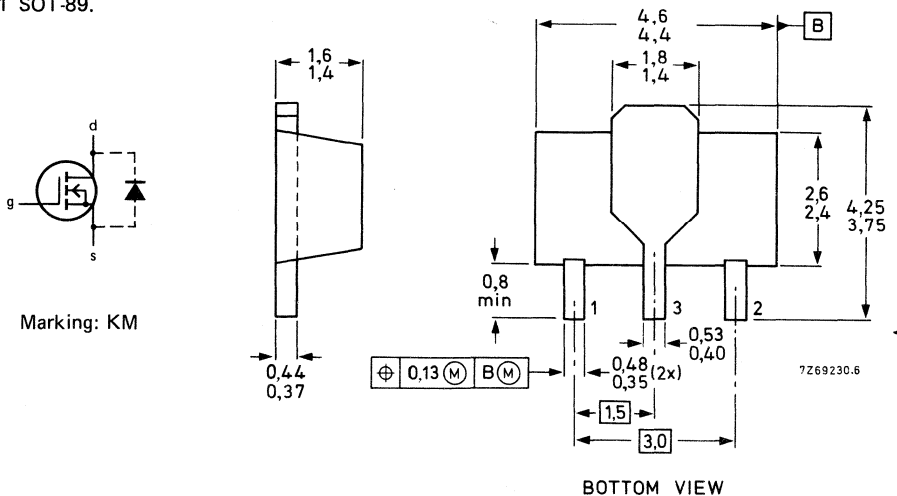
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GS}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	2,0 $\Omega$ 4,0 $\Omega$
Transfer admittance $I_D = 500\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	300 mS

**MECHANICAL DATA**

Dimensions in mm

Fig. 1 SOT-89.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GS0}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,5 A
Drain current (peak)	$I_{DM}$	max.	1,0 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-65 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

## THERMAL RESISTANCE

From junction to ambient *	$R_{th\ j-a}$	125 K/W
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## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	>	80 V
Drain-source leakage current $V_{DS} = 60\ \text{V}; V_{GS} = 0$	$I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $V_{GS} = 20\ \text{V}; V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $I_D = 500\ \text{mA}; V_{GS} = 10\ \text{V}$	$R_{DSon}$	typ. <	2,0 $\Omega$ 4,0 $\Omega$
Transfer admittance at $f = 1\ \text{kHz}$ $I_D = 500\ \text{mA}; V_{DS} = 15\ \text{V}$	$ y_{fs} $	typ.	300 mS
Input capacitance at $f = 1\ \text{MHz}$ $V_{DS} = 10\ \text{V}; V_{GS} = 0$	$C_{is}$	typ.	45 pF
Output capacitance at $f = 1\ \text{MHz}$ $V_{DS} = 10\ \text{V}; V_{GS} = 0$	$C_{os}$	typ.	30 pF
Feedback capacitance at $f = 1\ \text{MHz}$ $V_{DS} = 10\ \text{V}; V_{GS} = 0$	$C_{rs}$	typ.	8 pF
Switching times (see Figs 2 and 3) $I_D = 500\ \text{mA}; V_{DS} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$	$t_{on}$ $t_{off}$	< <	10 ns 15 ns

\* Transistors mounted on a substrate with surface area of 2,5 cm<sup>2</sup> and thickness of 0,7 mm.



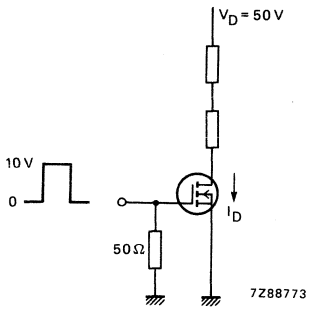


Fig. 2 Switching times test circuit.

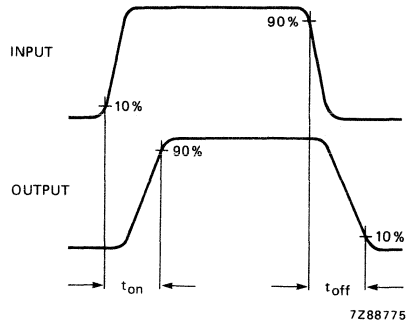


Fig. 3 Input and output waveforms.



## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line-transformer drivers.

**Features:**

- Direct interface to C-MOS, TTL. etc.
- High-speed switching
- No second breakdown

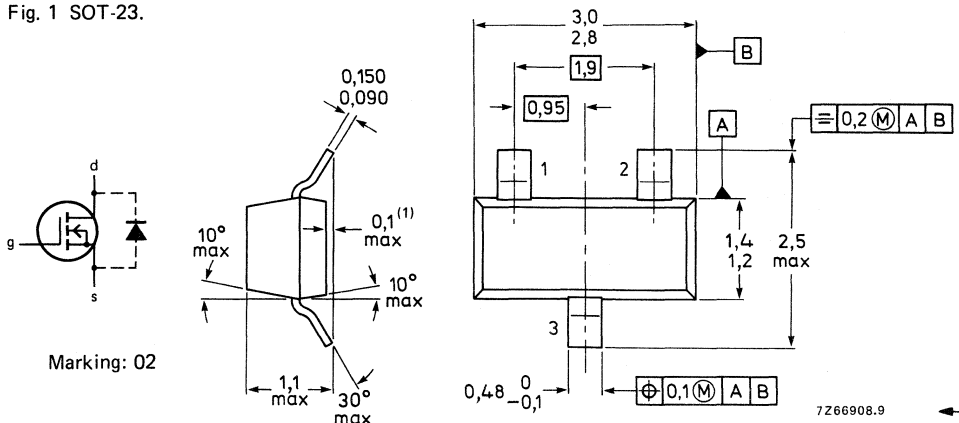
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	175 mA
Total power dissipation up to $T_{amb} = 25$ °C	$P_{tot}$	max.	300 mW
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DSon}$	typ.	7 $\Omega$ < 10 $\Omega$
Transfer admittance $I_D = 175$ mA; $V_{DS} = 5$ V; $f = 1$ kHz	$ y_{fs} $	typ.	150 mS

**MECHANICAL DATA**

Dimensions in mm

Fig. 1 SOT-23.



(1) Also available in 0,1 – 0,2 mm version.

TOP VIEW

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	175 mA
Drain current (peak)	$I_{DM}$	max.	600 mA
Total power dissipation up to $T_{amb} = 25$ °C *	$P_{tot}$	max.	300 mW
Storage temperature	$T_{stg}$	-65 to +150	°C
Junction temperature	$T_j$	max.	150 °C

**THERMAL RESISTANCE**

From junction to ambient *	$R_{th j-a}$	430	K/W
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**CHARACTERISTICS**

$T_j = 25$  °C unless otherwise specified

Drain-source breakdown voltage

$I_D = 100$   $\mu$ A;  $V_{GS} = 0$

$V_{(BR)DS}$	>	80	V
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Drain-source leakage current

$V_{DS} = 60$  V;  $V_{GS} = 0$

$I_{DSS}$	<	1,0	$\mu$ A
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Gate-source leakage current

$V_{GS} = 20$  V;  $V_{DS} = 0$

$I_{GSS}$	<	100	nA
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→ Gate-source cut-off voltage

$I_D = 1$  mA;  $V_{DS} = V_{GS}$

$V_{(P)GS}$	>	1,5	V
	<	3,5	V

Drain-source ON-resistance (see Fig. 4)

$I_D = 150$  mA;  $V_{GS} = 5$  V

$R_{DSon}$	typ.	7	$\Omega$
	<	10	$\Omega$

Transfer admittance at  $f = 1$  kHz

$I_D = 175$  mA;  $V_{DS} = 5$  V

$ y_{fs} $	typ.	150	mS
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Input capacitance at  $f = 1$  MHz

$V_{DS} = 10$  V;  $V_{GS} = 0$

$C_{is}$	typ.	15	pF
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Output capacitance at  $f = 1$  MHz

$V_{DS} = 10$  V;  $V_{GS} = 0$

$C_{os}$	typ.	13	pF
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Feedback capacitance at  $f = 1$  MHz

$V_{DS} = 10$  V;  $V_{GS} = 0$

$C_{rs}$	typ.	3	pF
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Switching times (see Figs 2 and 3)

$I_D = 175$  mA;  $V_{DS} = 50$  V;  $V_{GS} = 0$  to 10 V

$t_{on}$	typ.	4	ns
	<	10	ns

$t_{off}$	typ.	4	ns
	<	10	ns

\* Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0,5 mm.

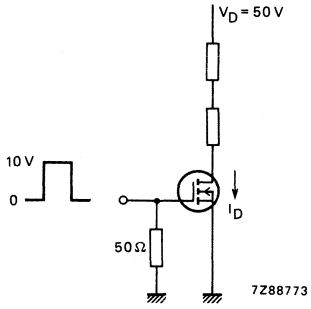


Fig. 2 Switching times test circuit.

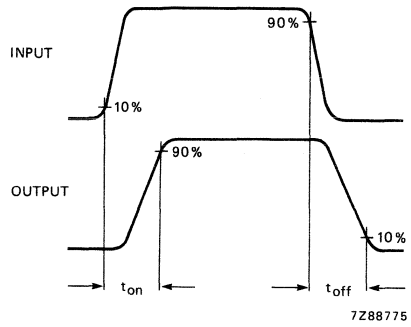


Fig. 3 Input and output waveforms.



## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT-89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

**Features :**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

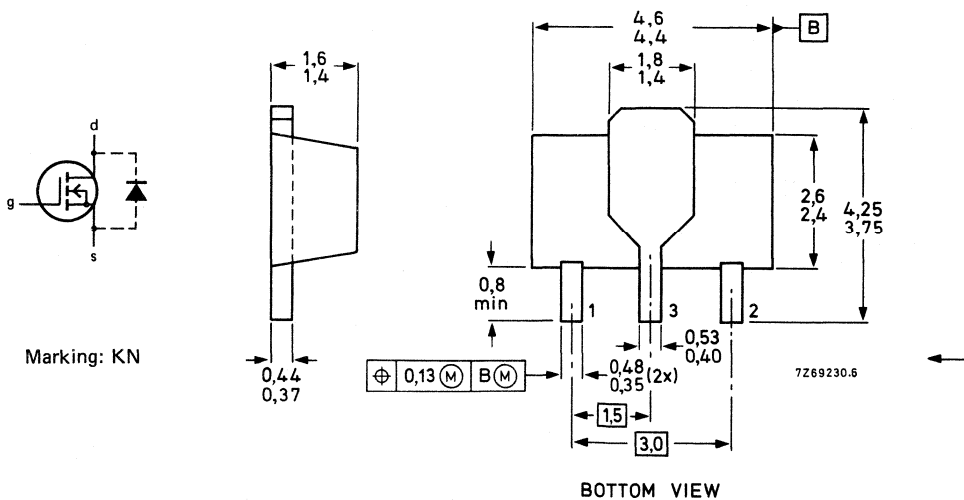
**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	6 $\Omega$ 12 $\Omega$
Transfer admittance $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	250 mS

**MECHANICAL DATA**

Dimensions in mm

Fig. 1 SOT-89.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	250 mA
Drain current (peak)	$I_{DM}$	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ *	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-65 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient *	$R_{th\ j-a}$		125 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	>	200 V
Drain-source leakage current $V_{DS} = 160\text{ V}; V_{GS} = 0$	$I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,8 V 2,8 V
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	6 $\Omega$ 12 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	250 mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{is}$	typ.	70 pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{os}$	typ.	20 pF
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	5 pF
Switching times (see Figs 2 and 3) $I_D = 250\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$	typ. <	4 ns 10 ns
	$t_{off}$	typ. <	15 ns 25 ns

\* Transistor mounted on a ceramic substrate with area of 2,5 cm<sup>2</sup> and thickness of 0,7 mm.



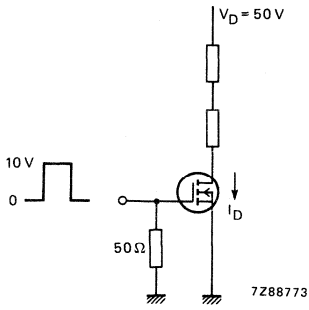


Fig. 2. Switching times test circuit.

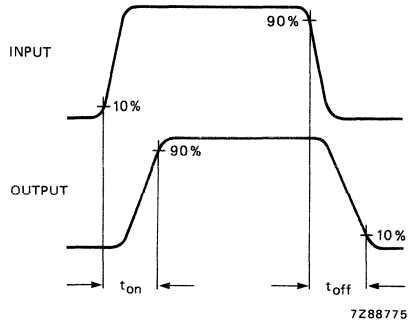


Fig. 3. Input and output waveforms.



## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

**Features:**

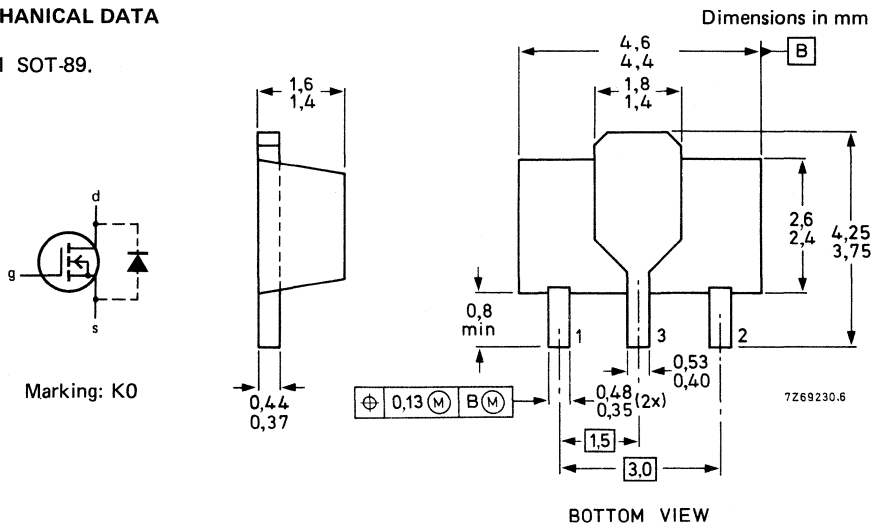
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Total power dissipation up to $T_{amb} = 25$ °C	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	$R_{DSon}$	typ.	7 $\Omega$ < 10 $\Omega$
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$ y_{fs} $	typ.	250 mS

**MECHANICAL DATA**

Fig. 1 SOT-89.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max. 180 V
Drain-source voltage (non repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max. 200 V
Gate-source voltage (open drain)	$V_{GSO}$	max. 20 V
Drain current (d.c.)	$I_D$	max. 300 mA
Drain current (peak)	$I_{DM}$	max. 800 mA
Total power dissipation up to $T_{amb} = 25$ °C *	$P_{tot}$	max. 1 W
Storage temperature	$T_{stg}$	-65 to +150 °C
Junction temperature	$T_j$	max. 150 °C

**THERMAL RESISTANCE**

From junction to ambient *	$R_{th\ j-a}$	125 K/W
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**CHARACTERISTICS**

$T_j = 25$  °C unless otherwise specified

Drain-source breakdown voltage

$I_D = 100 \mu A; V_{GS} = 0$

$V_{(BR)DS} > 180$  V

Drain-source leakage current

$V_{DS} = 120$  V;  $V_{GS} = 0$

$I_{DSS} < 10 \mu A$

Gate-source leakage current

$V_{GS} = 20$  V;  $V_{DS} = 0$

$I_{GSS} < 100$  nA

Gate threshold voltage

$I_D = 100 \mu A; V_{DS} = V_{GS}$

$V_{GS(th)} > 0,7$  V  
 $< 2,7$  V

Drain-source ON-resistance

$I_D = 15$  mA;  $V_{GS} = 3$  V

$R_{DSon}$  typ. 7  $\Omega$   
 $< 10$   $\Omega$

$I_D = 300$  mA;  $V_{GS} = 10$  V

$R_{DSon}$  typ. 6  $\Omega$

Transfer admittance at  $f = 1$  kHz

$I_D = 300$  mA;  $V_{DS} = 15$  V

$|y_{fs}|$  typ. 250 mS

Input capacitance at  $f = 1$  MHz

$V_{DS} = 10$  V;  $V_{GS} = 0$

$C_{is}$  typ. 50 pF

Output capacitance at  $f = 1$  MHz

$V_{DS} = 10$  V;  $V_{GS} = 0$

$C_{os}$  typ. 20 pF

Feedback capacitance at  $f = 1$  MHz

$V_{DS} = 10$  V;  $V_{GS} = 0$

$C_{rs}$  typ. 6 pF

Switching times (see Figs 2 and 3)

$I_D = 300$  mA;  $V_{DS} = 50$  V;  $V_{GS} = 0$  to 10 V

$t_{on} < 10$  ns  
 $t_{off} < 15$  ns

\* Transistors mounted on a ceramic substrate with area of 2,5 cm<sup>2</sup> and thickness of 0,7 mm.

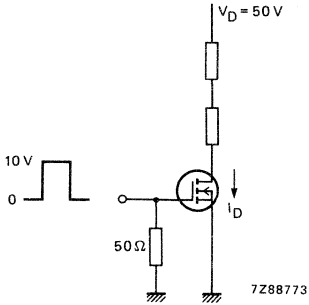


Fig. 2 Switching times test circuit.

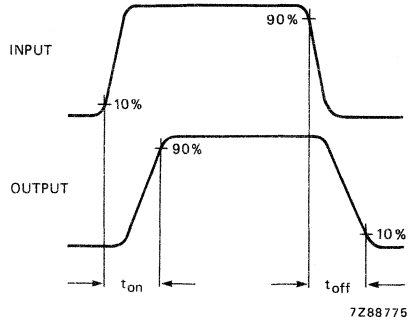


Fig. 3 Input and output waveforms.



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BST90

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

### Features

- Very low  $R_{DSon}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

### QUICK REFERENCE DATA

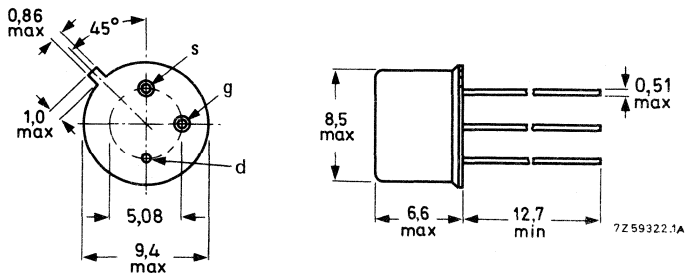
Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GS0}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,5 A
Total power dissipation up to $T_c = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	2,5 W
Drain-source ON-resistance $I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. max.	2 $\Omega$ 4 $\Omega$
Transfer admittance $I_D = 500\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	300 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.

Collector connected to case



Maximum lead diameter is guaranteed only for 12,7 mm.

Accessories: 56245 (distance disc).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	0,5 A
Drain current (peak)	$I_{DM}$	max.	1,0 A
Total power dissipation up to $T_c = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	2,5 W
Storage temperature	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

## THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125 K/W
From junction to case	$R_{th\ j-c}$	=	50 K/W

## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$I_D = 100\ \mu\text{A}; V_{GS} = 0$$

$$V_{(BR)DS} > 80\ \text{V}$$

Drain-source leakage current

$$V_{DS} = 60\ \text{V}; V_{GS} = 0$$

$$I_{DSS} < 10\ \mu\text{A}$$

Gate-source leakage current

$$V_{GS} = 20\ \text{V}; V_{DS} = 0$$

$$I_{GSS} < 100\ \text{nA}$$

Gate threshold voltage

$$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$$

$$V_{GS(th)} > 1,5\ \text{V}$$

$$< 3,5\ \text{V}$$

Drain-source ON-resistance (see Fig. 4)

$$I_D = 500\ \text{mA}; V_{GS} = 10\ \text{V}$$

$$R_{DSon} \text{ typ. } 2,0\ \Omega$$

$$< 4,0\ \Omega$$

Transfer admittance at  $f = 1\ \text{kHz}$

$$I_D = 500\ \text{mA}; V_{DS} = 15\ \text{V}$$

$$|y_{fs}| \text{ typ. } 300\ \text{mS}$$

Input capacitance at  $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{is} \text{ typ. } 45\ \text{pF}$$

Output capacitance at  $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{os} \text{ typ. } 30\ \text{pF}$$

Feedback capacitance at  $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{rs} \text{ typ. } 8\ \text{pF}$$

Switching times (see Figs 2 and 3)

$$I_D = 500\ \text{mA}; V_{DS} = 50\ \text{V}; V_{GS} = 0\ \text{to } 10\ \text{V}$$

$$t_{on} < 10\ \text{ns}$$

$$t_{off} < 15\ \text{ns}$$



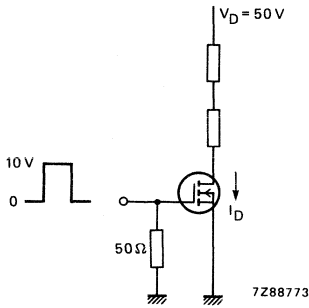


Fig. 2 Switching times test circuit.

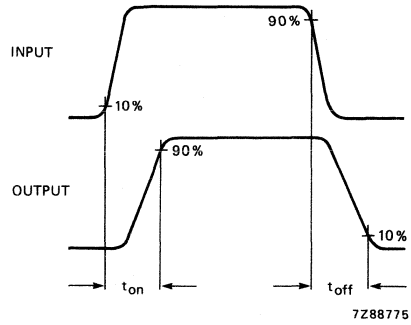


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

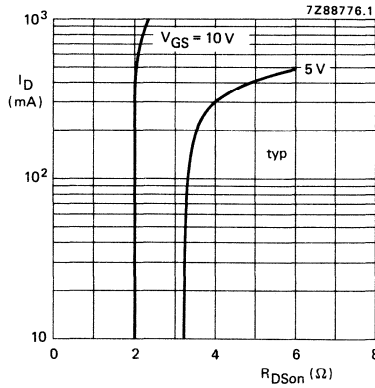


Fig. 4  $T_j = 25^\circ C$ .



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BST97

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-18 and designed for use as line current interrupter in telephone sets and for application in relay, high speed and line transformer drivers.

### Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

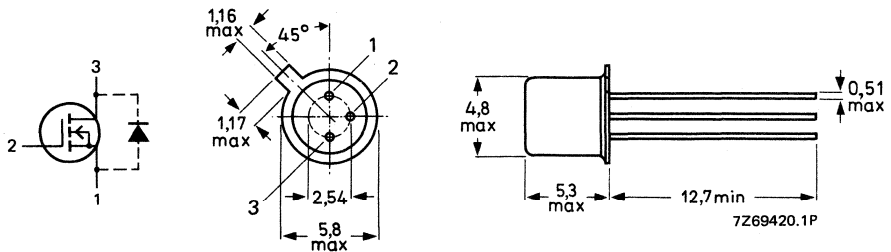
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Total power dissipation up to $T_C = 25$ °C	$P_{tot}$	max.	1,5 W
Drain-source ON-resistance $I_D = 300$ mA; $V_{GS} = 10$ V	$R_{DS(on)}$	typ.	6 $\Omega$
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$ y_{fs} $	typ.	250 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (d.c.)	$I_D$	max.	300 mA
Drain current (peak)	$I_{DM}$	max.	800 mA
Total power dissipation up to $T_{amb} = 25$ °C	$P_{tot}$	max.	0,4 W
Total power dissipation up to $T_C = 25$ °C	$P_{tot}$	max.	1,5 W
Storage temperature	$T_{stg}$		-65 to +150 °C
Junction temperature	$T_j$	max.	150 °C

**THERMAL RESISTANCE**

From junction to ambient	$R_{th\ j-a}$	310 K/W
From junction to case	$R_{th\ j-c}$	83 K/W

**CHARACTERISTICS**

$T_j = 25$  °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ $\mu$ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	180 V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	$I_{DSS}$	<	10 $\mu$ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	$I_{GSS}$	<	100 nA
Gate threshold voltage $I_D = 100$ $\mu$ A; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,7 V 2,7 V
Drain-source ON-resistance (see Fig. 4) $I_D = 15$ mA; $V_{GS} = 3$ V	$R_{DSon}$	typ. <	7 $\Omega$ 10 $\Omega$
$I_D = 300$ mA; $V_{GS} = 10$ V	$R_{DSon}$	typ.	6 $\Omega$
Transfer admittance at $f = 1$ kHz $I_D = 300$ mA; $V_{DS} = 15$ V	$ y_{fs} $	typ.	250 mS
Input capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{is}$	typ.	50 pF
Output capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{os}$	typ.	20 pF
Feedback capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	$C_{rs}$	typ.	6 pF
Switching times (see Figs 2 and 3) $I_D = 300$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	$t_{on}$ $t_{off}$	< <	10 ns 15 ns

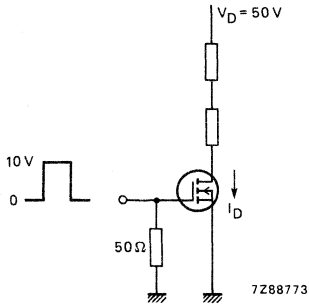


Fig. 2 Switching times test circuit.

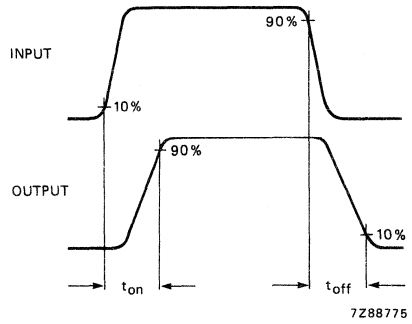


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

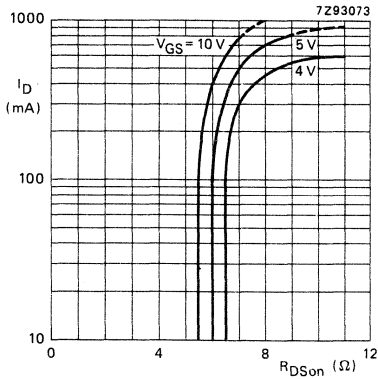


Fig. 4  $T_j = 25^\circ C$ ; typ. values.



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BST100

## P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

### Features:

- Very low  $R_{DSon}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

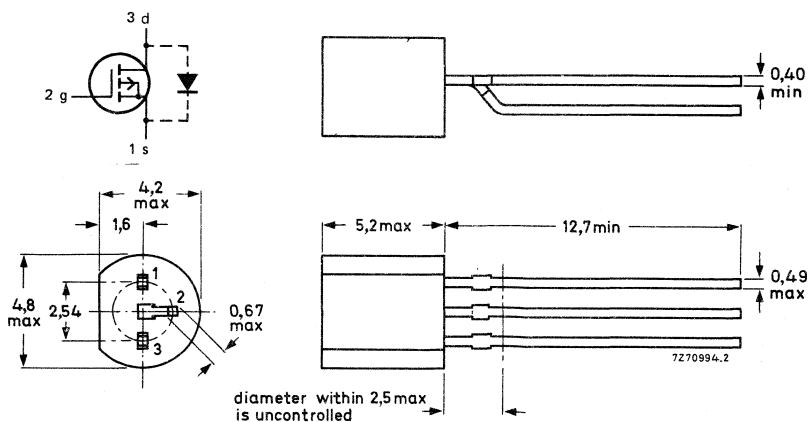
### QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ.	4,5 $\Omega$
		max.	6 $\Omega$
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	200 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GS0}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Drain current (peak)	$-I_{DM}$	max.	0,8 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-65 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

## THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$		125 K/W
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## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; -V_{GS} = 0$	$-V_{(BR)DS}$	>	60 V
Drain-source leakage current $-V_{DS} = 45\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	4,5 $\Omega$ 6 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	200 mS
Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{is}$	typ.	55 pF
Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{os}$	typ.	30 pF
Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	8 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_{DS} = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$ $t_{off}$	typ.	4 ns 20 ns

\* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.



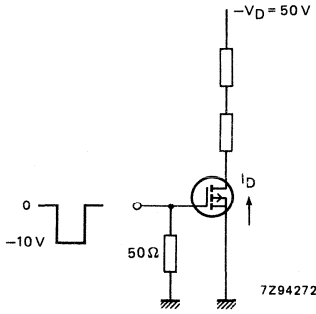


Fig. 2 Switching times test circuit.

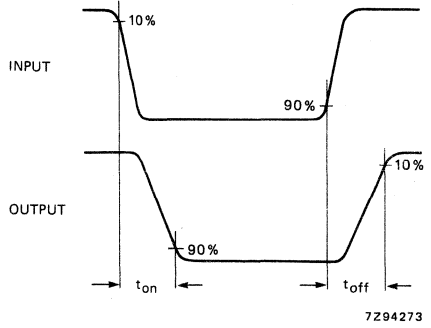


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BST110

## P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

### Features

- Very low  $R_{DSon}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

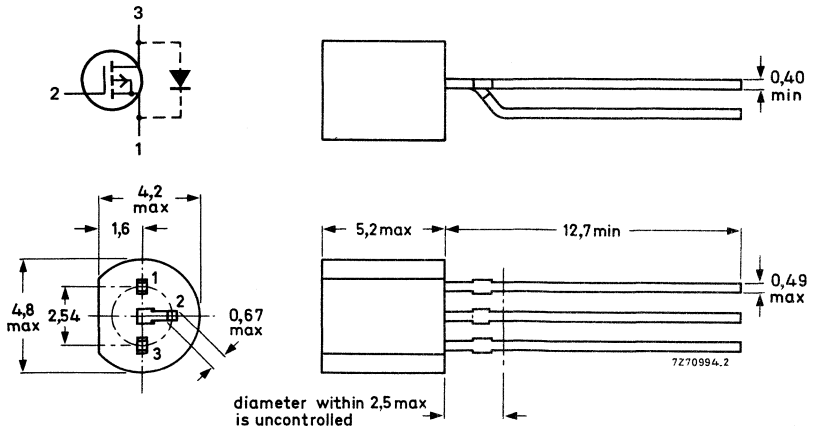
### QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage, open drain	$-V_{GS0}$	max.	20 V
Drain current, d.c.	$-I_D$	max.	0,25 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	0,83 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	7,5 $\Omega$ 10 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage, open drain	$-V_{GSO}$	max.	20 V
Drain current, d.c.	$-I_D$	max.	0,25 A
Drain current, peak	$-I_{DM}$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	0,83 W
Storage temperature	$T_{stg}$		$-65$ to $+150\text{ }^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient*	$R_{th\ j-a}$	=	150 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$-V_{(BR)DS}$	>	50 V
Drain-source leakage current $-V_{DS} = 40\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	>	1,5 V
		<	3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ.	7,5 $\Omega$
		<	10 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS

\* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

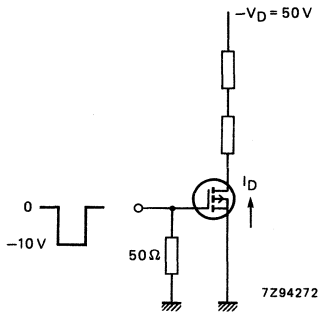


Fig. 2 Switching times test circuit.

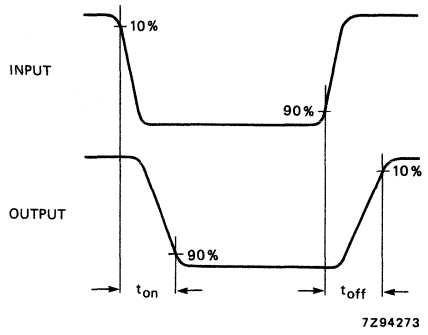


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BST120

## P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT-89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

### Features

- Very low  $R_{DSon}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

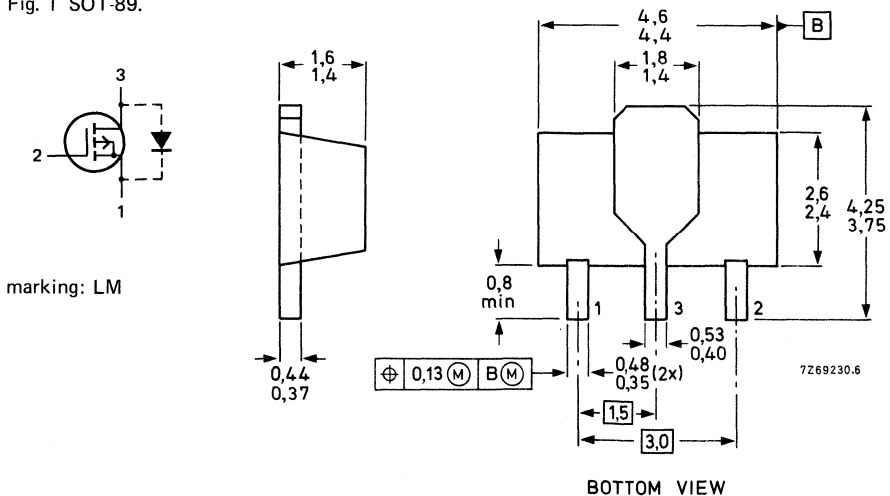
### QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ.	4,5 $\Omega$
		max.	6 $\Omega$
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	200 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Drain current (peak)	$-I_{DM}$	max.	0,8 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}^*$	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		$-65$ to $+150\text{ }^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient*	$R_{th\ j-a}$	=	125 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; -V_{GS} = 0$	$-V_{(BR)DS}$	>	60 V
Drain-source leakage current $-V_{DS} = 45\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	4,5 $\Omega$ 6 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	200 mS
Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{is}$	typ.	55 pF
Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{os}$	typ.	30 pF
Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	8 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_{DS} = 50\text{ V}; -V_{GS} = 0$ to $10\text{ V}$	$t_{on}$ $t_{off}$	typ. typ.	4 ns 20 ns

\* Transistor mounted on a ceramic substrate: area = 2,5 cm<sup>2</sup> and thickness = 0,7 mm.



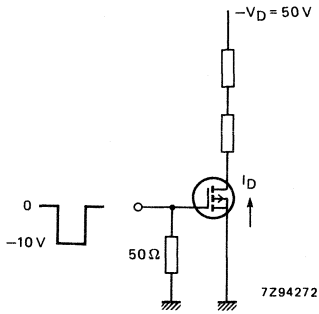


Fig. 2 Switching time test circuit.

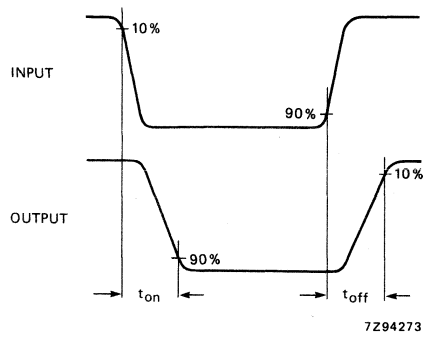


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BST122

## P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT-89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

### Features

- Very low  $R_{DSon}$
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

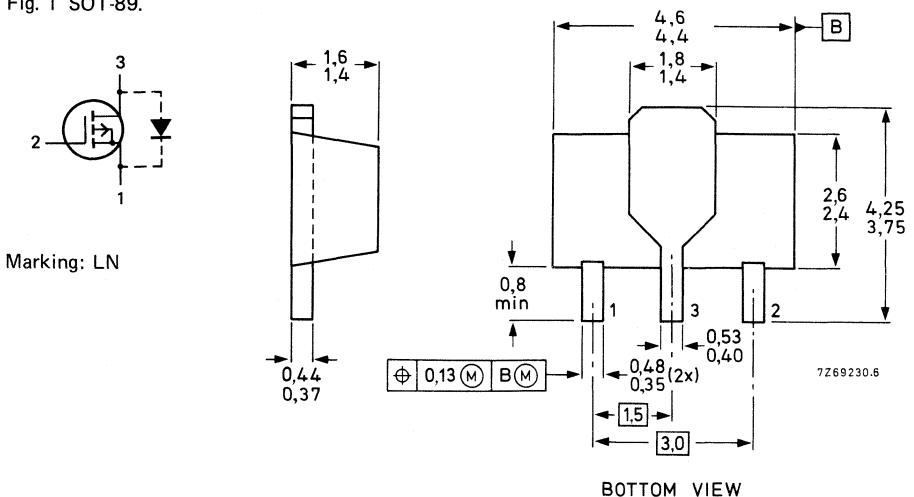
### QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. max.	7,5 $\Omega$ 10 $\Omega$
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	125 mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.



Marking: LN

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Drain current (peak)	$-I_{DM}$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		$-65$ to $+150\text{ }^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient*	$R_{th\ j-a}$	=	125 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; -V_{GS} = 0$	$-V_{(BR)DS}$	>	50 V
Drain-source leakage current $-V_{DS} = 1\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 $\mu\text{A}$
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	7,5 $\Omega$ 10 $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS
Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{is}$	typ.	55 pF
Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{os}$	typ.	30 pF
Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	8 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_{DS} = 50\text{ V}; -V_{GS} = 0$ to $10\text{ V}$	$t_{on}$ $t_{off}$	typ. typ.	4 ns 20 ns

\* Transistor mounted on a ceramic substrate: area = 2,5 cm<sup>2</sup>; thickness = 0,7 mm.

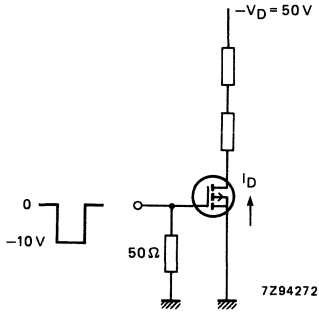


Fig. 2 Switching times test circuit.

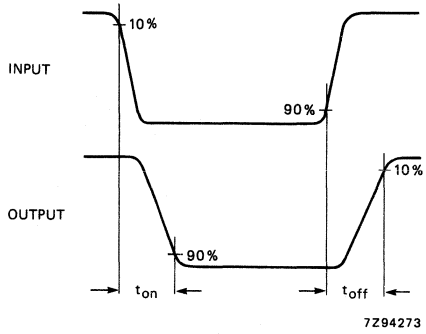


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA



## N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

## QUICK REFERENCE DATA

Drain-source resistance (on) at  $f = 1$  kHz

$$V_{DS} = 0; V_{GS} = 5 \text{ V}; V_{BS} = 0$$

$$r_{ds \text{ on}} < 50 \ \Omega$$

Drain-source resistance (off)

$$V_{DS} = 10 \text{ V}; -V_{GS} = 5 \text{ V}; V_{BS} = 0$$

$$r_{DS \text{ off}} > 10 \ \text{G}\Omega$$

Feedback capacitance at  $f = 1$  MHz

$$-V_{GS} = 5 \text{ V}; V_{DS} = 0; I_B = 0$$

$$C_{rs} < 0,5 \ \text{pF}$$

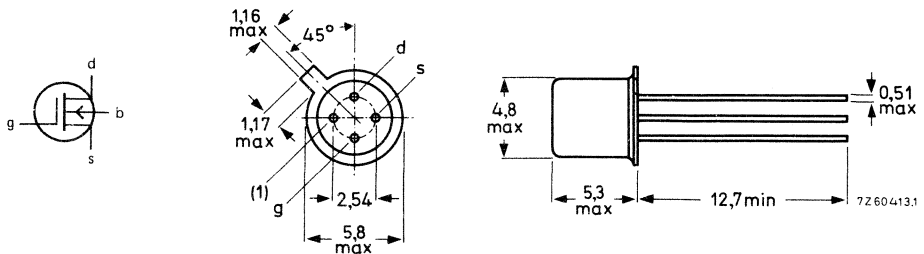
$$-V_{GD} = 5 \text{ V}; V_{SD} = 0; I_B = 0$$

$$C_{rd} < 0,5 \ \text{pF}$$

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = substrate connected to case.

Accessories: 56246 (distance disc).

## Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-substrate voltage	$V_{DB}$	max.	30 V
Source-substrate voltage	$V_{SB}$	max.	30 V
Gate-substrate voltage (continuous)	$V_{GB}$	max.	10 V
		min.	-10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0; f > 100 \text{ Hz}$	$V_{G-N}$	max.	15 V
		min.	-15 V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0; t < 10 \text{ ms}$	$V_{G-N}$	max.	50 V
		min.	-50 V

Currents

Drain current (peak value) $t_r = 20 \text{ ms}; \delta = 0,1$	$I_{DM}$	max.	50 mA
Source current (peak value) $t_r = 20 \text{ ms}; \delta = 0,1$	$I_{SM}$	max.	50 mA

Power dissipation

Total power dissipation up to $T_{amb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	200 mW
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Temperatures

Storage temperature	$T_{stg}$	-65 to +125	$^\circ\text{C}$
Junction temperature	$T_j$	max.	125 $^\circ\text{C}$

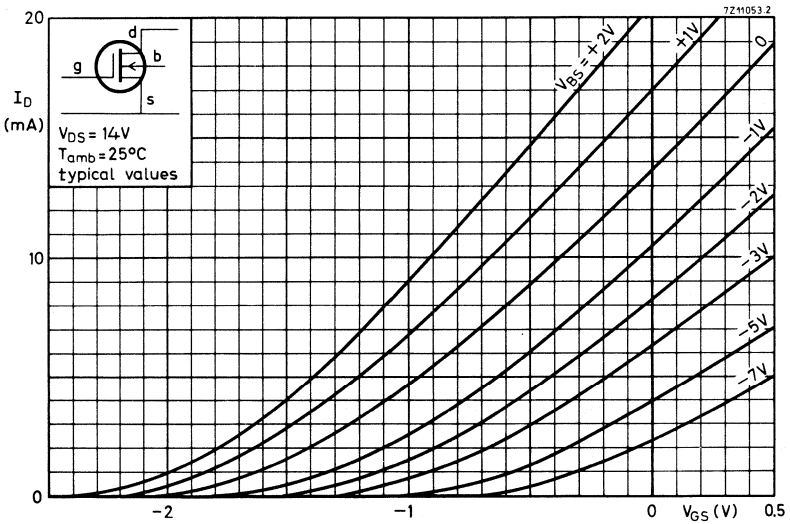
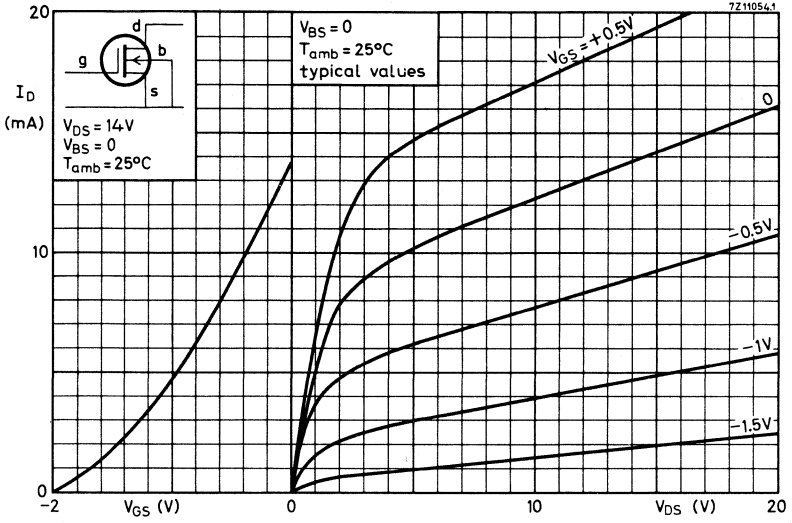
**THERMAL RESISTANCE**

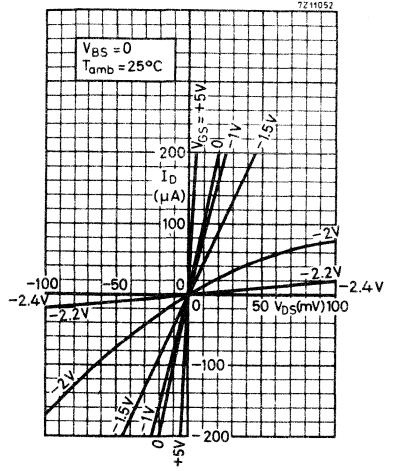
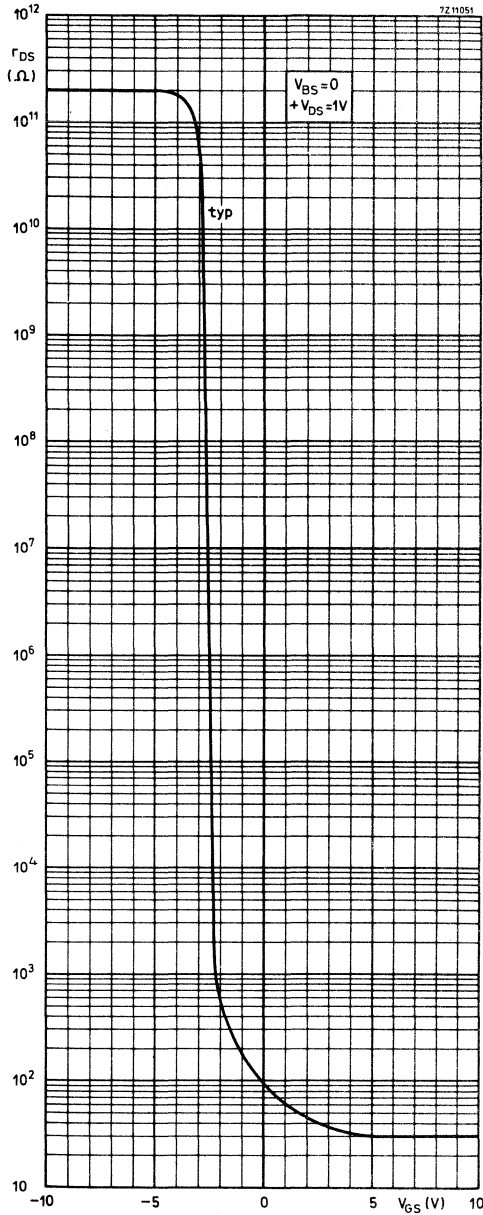
From junction to ambient in free air	$R_{th \text{ j-a}}$	=	0,5 $^\circ\text{C}/\text{mW}$
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**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specifiedDrain cut-off currents;  $V_{BS} = 0$  $V_{DS} = 10\text{ V}$ ;  $-V_{GS} = 5\text{ V}$   $I_{DSX} < 1\text{ nA}$  $V_{DS} = 10\text{ V}$ ;  $-V_{GS} = 5\text{ V}$ ;  $T_j = 125\text{ }^\circ\text{C}$   $I_{DSX} < 1\text{ }\mu\text{A}$ Source cut-off currents;  $V_{BD} = 0$  $V_{SD} = 10\text{ V}$ ;  $-V_{GD} = 5\text{ V}$   $I_{SDX} < 1\text{ nA}$  $V_{SD} = 10\text{ V}$ ;  $-V_{GD} = 5\text{ V}$ ;  $T_j = 125\text{ }^\circ\text{C}$   $I_{SDX} < 1\text{ }\mu\text{A}$ Gate currents;  $V_{BS} = 0$  $-V_{GS} = 10\text{ V}$ ;  $V_{DS} = 0$   $-I_{GSS} < 10\text{ pA}$  $V_{GS} = 10\text{ V}$ ;  $V_{DS} = 0$   $I_{GSS} < 10\text{ pA}$  $-V_{GS} = 10\text{ V}$ ;  $V_{DS} = 0$ ;  $T_j = 125\text{ }^\circ\text{C}$   $-I_{GSS} < 200\text{ pA}$  $V_{GS} = 10\text{ V}$ ;  $V_{DS} = 0$ ;  $T_j = 125\text{ }^\circ\text{C}$   $I_{GSS} < 200\text{ pA}$ Bulk currents;  $V_{GB} = 0$  $-V_{BD} = 30\text{ V}$ ;  $I_S = 0$   $-I_{BDO} < 10\text{ }\mu\text{A}$  $-V_{BS} = 30\text{ V}$ ;  $I_D = 0$   $-I_{BSO} < 10\text{ }\mu\text{A}$ Drain-source resistance (on) at  $f = 1\text{ kHz}$ ;  $V_{BS} = 0$  $V_{GS} = 0$ ;  $V_{DS} = 0$   $r_{dson} < 100\text{ }\Omega$  $V_{GS} = 0$ ;  $V_{DS} = 0$ ;  $T_j = 125\text{ }^\circ\text{C}$   $r_{dson} < 150\text{ }\Omega$  $+V_{GS} = 5\text{ V}$ ;  $V_{DS} = 0$   $r_{dson} < 50\text{ }\Omega$ Drain-source resistance (off) $-V_{GS} = 5\text{ V}$ ;  $V_{DS} = 10\text{ V}$ ;  $V_{BS} = 0$   $r_{DSoff} > 10\text{ G}\Omega$ Feedback capacitances at  $f = 1\text{ MHz}$  $-V_{GS} = 5\text{ V}$ ;  $V_{DS} = 0$ ;  $I_B = 0$   $C_{rs} < 0,5\text{ pF}$  $-V_{GD} = 5\text{ V}$ ;  $V_{SD} = 0$ ;  $I_B = 0$   $C_{rd} < 0,5\text{ pF}$ Gate to all other terminals capacitance at  $f = 1\text{ MHz}$  $-V_{GB} = 5\text{ V}$ ;  $V_{SB} = V_{DB} = 0$   $C_{g-n} < 6\text{ pF}$

# BSV81







# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

2N6659  
2N6660  
2N6661

## N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

### Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low  $R_{DSon}$

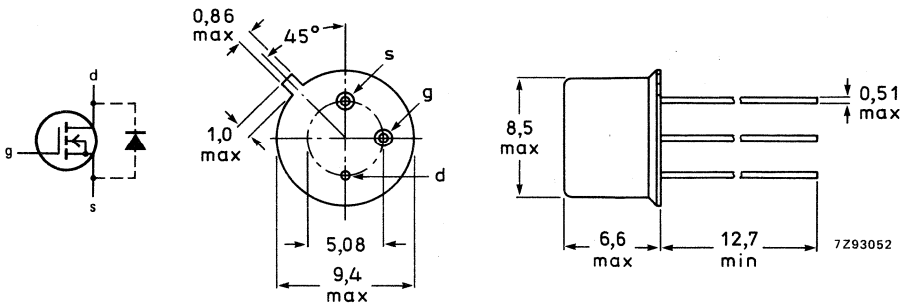
### QUICK REFERENCE DATA

		2N6659	2N6660	2N6661	
Drain-source voltage	$V_{DS}$	max. 35	60	90	V
Gate-source voltage (open drain)	$V_{GSO}$	max. 20	20	20	V
Drain current (d.c.)	$I_D$	max. 1,4	1,1	0,9	A
Total power dissipation up to $T_c = 25^\circ\text{C}$	$P_{tot}$	max. 6,25	6,25	6,25	W
Drain-source ON-resistance $I_D = 1,0\text{ A}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. 0,9 < 1,8	1,4 3,0	1,9 4,0	$\Omega$ $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 0,5\text{ A}; V_{DS} = 25\text{ V}$	$ y_{fs} $	> 170	170	170	mS

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.



Maximum lead diameter is guaranteed only for 12,7 mm

Accessories: 56245 (distance disc).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N6659	2N6660	2N6661	
Drain-source voltage	$V_{DS}$	max.	35	60	90	V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20	20	20	V
Drain current (d.c.)	$I_D$	max.	1,4	1,1	0,9	A
Drain current (peak)*	$I_{DM}$	max.		3,0		A
Total power dissipation up to $T_c = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.		6,25		W
Storage temperature	$T_{stg}$			-65 to + 150		$^\circ\text{C}$
Junction temperature	$T_j$	max.		150		$^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to case	$R_{th\ j-c}$			20		K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified .

			2N6659	2N6660	2N6661	
Drain-source breakdown voltage $I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DSS}$	>	35	60	90	V
Drain-source leakage current at $V_{DS} = V_{DSmax}; V_{GS} = 0$	$I_{DSS}$	<	10	10	10	$\mu\text{A}$
Gate-source leakage current at $V_{GS} = 15\text{ V}; V_{DS} = 0$	$I_{GSS}$	<	100	100	100	nA
Gate threshold voltage $I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,8 2,0	0,8 2,0	0,8 2,0	V V
ON-state drain current $V_{DS} = 25\text{ V}; V_{GS} = 10\text{ V}$	$I_{D(on)}$	> typ.	1,0 2,0	1,0 2,0	1,0 2,0	A A
Drain-source ON-resistance $I_D = 0,3\text{ A}; V_{GS} = 5\text{ V}$	$R_{DSon}$	typ. <	1,5 5,0	1,8 5,0	2,4 5,3	$\Omega$ $\Omega$
$I_D = 1,0\text{ A}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. <	0,9 1,8	1,4 3,0	1,9 4,0	$\Omega$ $\Omega$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 0,5\text{ A}; V_{DS} = 25\text{ V}$	$ y_{fs} $	>	170	170	170	mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 25\text{ V}; V_{GS} = 0$	$C_{iss}$	<	60	60	60	pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 25\text{ V}; V_{GS} = 0$	$C_{oss}$	<	50	40	40	pF

\* Pulse conditions:  $t_p \leq 300\text{ }\mu\text{s}; \delta = 0,01.$

N-channel vertical D-MOS transistor

2N6659  
2N6660  
2N6661

		2N6659	2N6660	2N6661
Feedback capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 25 \text{ V}; V_{GS} = 0$				
$C_{rss}$	<	10	10	10 pF
Switching times $I_D = 1,0 \text{ A}; V_{DS} = 25 \text{ V};$ $V_{GS} = 0 \text{ to } 20 \text{ V}$				
$t_{on}$	<	10	10	10 ns
$t_{off}$	<	20	20	20 ns

DEVELOPMENT DATA

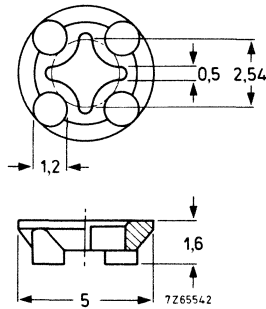
DISTANCE DISC

MECHANICAL DATA

Dimensions in mm

Fig. 1 56246 for TO-18 or TO-72.

Insulating material.



TEMPERATURE

Maximum permissible temperature

T max. 100 °C



## INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

type no.	book	section	type no.	book	section	type no.	book	section
BA220	S1	SD	BAS29	S7/S1	Mm/SD	BAV101	S7/S1	Mm/SD
BA221	S1	SD	BAS31	S7/S1	Mm/SD	BAV102	S7/S1	Mm/SD
BA223	S1	T	BAS32	S7/S1	Mm/SD	BAV103	S7/S1	Mm/SD
BA281	S1	SD	BAS35	S7/S1	Mm/SD	BAW56	S7/S1	Mm/SD
BA314	S1	Vrg	BAS45	S1	SD	BAW62	S1	SD
BA315	S1	Vrg	BAS56	S1	SD	BAX12	S1	SD
BA316	S1	SD	BAT17	S7/S1	Mm/T	BAX14	S1	SD
BA317	S1	SD	BAT18	S7/S1	Mm/T	BAX18	S1	SD
BA318	S1	SD	BAT54	S1	SD	BAY80	S1	SD
BA423	S1	T	BAT74	S1	SD	BB112	S1	T
BA480	S1	T	BAT81	S1	T	BB119	S1	T
BA481	S1	T	BAT82	S1	T	BB130	S1	T
BA482	S1	T	BAT83	S1	T	BB204B	S1	T
BA483	S1	T	BAT85	S1	T	BB204G	S1	T
BA484	S1	T	BAT86	S1	T	BB212	S1	T
BA682	S1	T	BAV10	S1	SD	BB405B	S1	T
BA683	S1	T	BAV18	S1	SD	BB417	S1	T
BAS11	S1	SD	BAV19	S1	SD	BB809	S1	T
BAS15	S1	SD	BAV20	S1	SD	BB909A	S1	T
BAS16	S7/S1	Mm/SD	BAV21	S1	SD	BB909B	S1	T
BAS17	S7/S1	Mm/Vrg	BAV23	S7/S1	Mm/SD	BBY31	S7/S1	Mm/T
BAS19	S7/S1	Mm/SD	BAV45	S1	Sp	BBY40	S7/S1	Mm/T
BAS20	S7/S1	Mm/SD	BAV70	S7/S1	Mm/SD	BC107	S3	Sm
BAS21	S7/S1	Mm/SD	BAV99	S7/S1	Mm/SD	BC108	S3	Sm
BAS28	S7/S1	Mm/SD	BAV100	S7/S1	Mm/SD	BC109	S3	Sm

Mm = Microminiature semiconductors  
for hybrid circuits  
SD = Small-signal diodes

Sp = Special diodes  
T = Tuner diodes  
Vrg = Voltage regulator diodes  
Sm = Small-signal transistors

# INDEX

type no.	book	section	type no.	book	section	type no.	book	section
BC140	S3	Sm	BC818	S7	Mm	BCX51	S7	Mm
BC141	S3	Sm	BC846	S7	Mm	BCX52	S7	Mm
BC146	S3	Sm	BC847	S7	Mm	BCX53	S7	Mm
BC160	S3	Sm	BC848	S7	Mm	BCX54	S7	Mm
BC161	S3	Sm	BC849	S7	Mm	BCX55	S7	Mm
BC177	S3	Sm	BC850	S7	Mm	BCX56	S7	Mm
BC178	S3	Sm	BC856	S7	Mm	BCX68	S7	Mm
BC179	S3	Sm	BC857	S7	Mm	BCX69	S7	Mm
BC200	S3	Sm	BC858	S7	Mm	BCX70*	S7	Mm
BC264A	S5	FET	BC859	S7	Mm	BCX71*	S7	Mm
BC264B	S5	FET	BC860	S7	Mm	BCY56	S3	Sm
BC264C	S5	FET	BC868	S7	Mm	BCY57	S3	Sm
BC264D	S5	FET	BC869	S7	Mm	BCY58	S3	Sm
BC327;A	S3	Sm	BCF29;R	S7	Mm	BCY59	S3	Sm
BC328	S3	Sm	BCF30;R	S7	Mm	BCY70	S3	Sm
BC337;A	S3	Sm	BCF32;R	S7	Mm	BCY71	S3	Sm
BC338	S3	Sm	BCF33;R	S7	Mm	BCY72	S3	Sm
BC368	S3	Sm	BCF70;R	S7	Mm	BCY78	S3	Sm
BC369	S3	Sm	BCF81;R	S7	Mm	BCY79	S3	Sm
BC375	S3	Sm	BCV61	S7	Mm	BCY87	S3	Sm
BC376	S3	Sm	BCV62	S7	Mm	BCY88	S3	Sm
BC546	S3	Sm	BCV71;R	S7	Mm	BCY89	S3	Sm
BC547	S3	Sm	BCV72;R	S7	Mm	BD131	S4a	P
BC548	S3	Sm	BCW29;R	S7	Mm	BD132	S4a	P
BC549	S3	Sm	BCW30;R	S7	Mm	BD135	S4a	P
BC550	S3	Sm	BCW31;R	S7	Mm	BD136	S4a	P
BC556	S3	Sm	BCW32;R	S7	Mm	BD137	S4a	P
BC557	S3	Sm	BCW33;R	S7	Mm	BD138	S4a	P
BC558	S3	Sm	BCW60*	S7	Mm	BD139	S4a	P
BC559	S3	Sm	BCW61*	S7	Mm	BD140	S4a	P
BC560	S3	Sm	BCW69;R	S7	Mm	BD201	S4a	P
BC635	S3	Sm	BCW70;R	S7	Mm	BD202	S4a	P
BC636	S3	Sm	BCW71;R	S7	Mm	BD203	S4a	P
BC637	S3	Sm	BCW72;R	S7	Mm	BD204	S4a	P
BC638	S3	Sm	BCW81;R	S7	Mm	BD226	S4a	P
BC639	S3	Sm	BCW89;R	S7	Mm	BD227	S4a	P
BC640	S3	Sm	BCX17;R	S7	Mm	BD228	S4a	P
BC807	S7	Mm	BCX18;R	S7	Mm	BD229	S4a	P
BC808	S7	Mm	BCX19;R	S7	Mm	BD230	S4a	P
BC817	S7	Mm	BCX20;R	S7	Mm	BD231	S4a	P

\* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors  
for hybrid circuits

P = Low-frequency power transistors

Sm = Small-signal transistors

type no.	book	section	type no.	book	section	type no.	book	section
BD233	S4a	P	BD433	S4a	P	BD843	S4a	P
BD234	S4a	P	BD434	S4a	P	BD844	S4a	P
BD235	S4a	P	BD435	S4a	P	BD845	S4a	P
BD236	S4a	P	BD436	S4a	P	BD846	S4a	P
BD237	S4a	P	BD437	S4a	P	BD847	S4a	P
BD238	S4a	P	BD438	S4a	P	BD848	S4a	P
BD239	S4a	P	BD645	S4a	P	BD849	S4a	P
BD239A	S4a	P	BD646	S4a	P	BD850	S4a	P
BD239B	S4a	P	BD647	S4a	P	BD933	S4a	P
BD239C	S4a	P	BD648	S4a	P	BD934	S4a	P
BD240	S4a	P	BD649	S4a	P	BD935	S4a	P
BD240A	S4a	P	BD650	S4a	P	BD936	S4a	P
BD240B	S4a	P	BD651	S4a	P	BD937	S4a	P
BD240C	S4a	P	BD652	S4a	P	BD938	S4a	P
BD241	S4a	P	BD675	S4a	P	BD939	S4a	P
BD241A	S4a	P	BD676	S4a	P	BD940	S4a	P
BD241B	S4a	P	BD677	S4a	P	BD941	S4a	P
BD241C	S4a	P	BD678	S4a	P	BD942	S4a	P
BD242	S4a	P	BD679	S4a	P	BD943	S4a	P
BD242A	S4a	P	BD680	S4a	P	BD944	S4a	P
BD242B	S4a	P	BD681	S4a	P	BD945	S4a	P
BD242C	S4a	P	BD682	S4a	P	BD946	S4a	P
BD243	S4a	P	BD683	S4a	P	BD947	S4a	P
BD243A	S4a	P	BD684	S4a	P	BD948	S4a	P
BD243B	S4a	P	BD813	S4a	P	BD949	S4a	P
BD243C	S4a	P	BD814	S4a	P	BD950	S4a	P
BD244	S4a	P	BD815	S4a	P	BD951	S4a	P
BD244A	S4a	P	BD816	S4a	P	BD952	S4a	P
BD244B	S4a	P	BD817	S4a	P	BD953	S4a	P
BD244C	S4a	P	BD818	S4a	P	BD954	S4a	P
BD329	S4a	P	BD825	S4a	P	BD955	S4a	P
BD330	S4a	P	BD826	S4a	P	BD956	S4a	P
BD331	S4a	P	BD827	S4a	P	BDT20	S4a	P
BD332	S4a	P	BD828	S4a	P	BDT21	S4a	P
BD333	S4a	P	BD829	S4a	P	BDT29	S4a	P
BD334	S4a	P	BD830	S4a	P	BDT29A	S4a	P
BD335	S4a	P	BD839	S4a	P	BDT29B	S4a	P
BD336	S4a	P	BD840	S4a	P	BDT29C	S4a	P
BD337	S4a	P	BD841	S4a	P	BDT30	S4a	P
BD338	S4a	P	BD842	S4a	P	BDT30A	S4a	P

P = Low-frequency power transistors

# INDEX

type no.	book	section	type no.	book	section	type no.	book	section
BDT30B	S4a	P	BDT65B	S4a	P	BDX43	S4a	P
BDT30C	S4a	P	BDT65C	S4a	P	BDX44	S4a	P
BDT31	S4a	P	BDT91	S4a	P	BDX45	S4a	P
BDT31A	S4a	P	BDT92	S4a	P	BDX46	S4a	P
BDT31B	S4a	P	BDT93	S4a	P	BDX47	S4a	P
BDT31C	S4a	P	BDT94	S4a	P	BDX62	S4a	P
BDT32	S4a	P	BDT95	S4a	P	BDX62A	S4a	P
BDT32A	S4a	P	BDT96	S4a	P	BDX62B	S4a	P
BDT32B	S4a	P	BDV64	S4a	P	BDX62C	S4a	P
BDT32C	S4a	P	BDV64A	S4a	P	BDX63	S4a	P
BDT41	S4a	P	BDV64B	S4a	P	BDX63A	S4a	P
BDT41A	S4a	P	BDV64C	S4a	P	BDX63B	S4a	P
BDT41B	S4a	P	BDV65	S4a	P	BDX63C	S4a	P
BDT41C	S4a	P	BDV65A	S4a	P	BDX64	S4a	P
BDT42	S4a	P	BDV65B	S4a	P	BDX64A	S4a	P
BDT42A	S4a	P	BDV65C	S4a	P	BDX64B	S4a	P
BDT42B	S4a	P	BDV66A	S4a	P	BDX64C	S4a	P
BDT42C	S4a	P	BDV66B	S4a	P	BDX65	S4a	P
BDT60	S4a	P	BDV66C	S4a	P	BDX65A	S4a	P
BDT60A	S4a	P	BDV66D	S4a	P	BDX65B	S4a	P
BDT60B	S4a	P	BDV67A	S4a	P	BDX65C	S4a	P
BDT60C	S4a	P	BDV67B	S4a	P	BDX66	S4a	P
BDT61	S4a	P	BDV67C	S4a	P	BDX66A	S4a	P
BDT61A	S4a	P	BDV67D	S4a	P	BDX66B	S4a	P
BDT61B	S4a	P	BDV91	S4a	P	BDX66C	S4a	P
BDT61C	S4a	P	BDV92	S4a	P	BDX67	S4a	P
BDT62	S4a	P	BDV93	S4a	P	BDX67A	S4a	P
BDT62A	S4a	P	BDV94	S4a	P	BDX67B	S4a	P
BDT62B	S4a	P	BDV95	S4a	P	BDX67C	S4a	P
BDT62C	S4a	P	BDV96	S4a	P	BDX68	S4a	P
BDT63	S4a	P	BDW55	S4a	P	BDX68A	S4a	P
BDT63A	S4a	P	BDW56	S4a	P	BDX68B	S4a	P
BDT63B	S4a	P	BDW57	S4a	P	BDX68C	S4a	P
BDT63C	S4a	P	BDW58	S4a	P	BDX69	S4a	P
BDT64	S4a	P	BDW59	S4a	P	BDX69A	S4a	P
BDT64A	S4a	P	BDW60	S4a	P	BDX69B	S4a	P
BDT64B	S4a	P	BDX35	S4a	P	BDX69C	S4a	P
BDT64C	S4a	P	BDX36	S4a	P	BDX77	S4a	P
BDT65	S4a	P	BDX37	S4a	P	BDX78	S4a	P
BDT65A	S4a	P	BDX42	S4a	P	BDX91	S4a	P

P = Low-frequency power transistors

type no.	book	section	type no.	book	section	type no.	book	section
BDX92	S4a	P	BF471	S4b	HVP	BF960	S5	FET
BDX93	S4a	P	BF472	S4b	HVP	BF964	S5	FET
BDX94	S4a	P	BF483	S3	Sm	BF966	S5	FET
BDX95	S4a	P	BF485	S3	Sm	BF967	S3	Sm
BDX96	S4a	P	BF487	S3	Sm	BF970	S3	Sm
BDY90	S4a	P	BF494	S3	Sm	BF979	S3	Sm
BDY90A	S4a	P	BF495	S3	Sm	BF980	S5	FET
BDY91	S4a	P	BF496	S3	Sm	BF981	S5	FET
BDY92	S4a	P	BF510	S7/S5	Mm/FET	BF982	S5	FET
BF198	S3	Sm	BF511	S7/S5	Mm/FET	BF989	S7/S5	Mm/FET
BF199	S3	Sm	BF512	S7/S5	Mm/FET	BF990	S7/S5	Mm/FET
BF240	S3	Sm	BF513	S7/S5	Mm/FET	BF991	S7/S5	Mm/FET
BF241	S3	Sm	BF536	S7	Mm	BF992	S7/S5	Mm/FET
BF245A	S5	FET	BF550;R	S7	Mm	BF994	S7/S5	Mm/FET
BF245B	S5	FET	BF569	S7	Mm	BF996	S7/S5	Mm/FET
BF245C	S5	FET	BF579	S7	Mm	BFG23	S10	WBT
BF247A	S5	FET	BF620	S7	Mm	BFG32	S10	WBT
BF247B	S5	FET	BF621	S7	Mm	BFG34	S10	WBT
BF247C	S5	FET	BF622	S7	Mm	BFG51	S10	WBT
BF256A	S5	FET	BF623	S7	Mm	BFG65	S10	WBT
BF256B	S5	FET	BF660;R	S7	Mm	BFG90A	S10	WBT
BF256C	S5	FET	BF689K	S10	WBT	BFG91A	S10	WBT
BF324	S3	Sm	BF763	S10	WBT	BFG96	S10	WBT
BF370	S3	Sm	BF767	S7	Mm	BFP90A	S10	WBT
BF410A	S5	FET	BF819	S4b	HVP	BFP91A	S10	WBT
BF410B	S5	FET	BF820	S7	Mm	BFP96	S10	WBT
BF410C	S5	FET	BF821	S7	Mm	BFQ10	S5	FET
BF410D	S5	FET	BF822	S7	Mm	BFQ11	S5	FET
BF419	S4b	HVP	BF823	S7	Mm	BFQ12	S5	FET
BF420	S3	Sm	BF824	S7	Mm	BFQ13	S5	FET
BF421	S3	Sm	BF857	S4b	HVP	BFQ14	S5	FET
BF422	S3	Sm	BF858	S4b	HVP	BFQ15	S5	FET
BF423	S3	Sm	BF859	S4b	HVP	BFQ16	S5	FET
BF450	S3	Sm	BF869	S4b	HVP	BFQ17	S7	Mm
BF451	S3	Sm	BF870	S4b	HVP	BFQ18A	S7	Mm
BF457	S4b	HVP	BF871	S4b	HVP	BFQ19	S7	Mm
BF458	S4b	HVP	BF872	S4b	HVP	BFQ22S	S10	WBT
BF459	S4b	HVP	BF926	S3	Sm	BFQ23	S10	WBT
BF469	S4b	HVP	BF936	S3	Sm	BFQ23C	S10	WBT
BF470	S4b	HVP	BF939	S3	Sm	BFQ24	S10	WBT

FET = Field-effect transistors

HVP = High-voltage power transistors

Mm = Microminiature semiconductors

for hybrid circuits

P = Low-frequency power transistors

Sm = Small-signal transistors

WBT = Wideband hybrid IC transistors

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type no.	book	section	type no.	book	section	type no.	book	section
BFQ32	S10	WBT	BFS18;R	S7	Mm	BG2097	S1	RT
BFQ32C	S10	WBT	BFS19;R	S7	Mm	BGD102	S10	WBM
BFQ32S	S10	WBT	BFS20;R	S7	Mm	BGD102E	S10	WBM
BFQ33	S10	WBT	BFS21	S5	FET	BGD104	S10	WBM
BFQ34	S10	WBT	BFS21A	S5	FET	BGD104E	S10	WBM
BFQ34T	S10	WBT	BFS22A	S6	RFP	BGX11*	S2b	ThM
BFQ42	S6	RFP	BFS23A	S6	RFP	BGX12*	S2b	ThM
BFQ43	S6	RFP	BFT24	S10	WBT	BGX13*	S2b	ThM
BFQ51	S10	WBT	BFT25;R	S7	Mm	BGX14*	S2b	ThM
BFQ51C	S10	WBT	BFT44	S3	Sm	BGX15*	S2b	ThM
BFQ52	S10	WBT	BFT45	S3	Sm	BGX17*	S2b	ThM
BFQ53	S10	WBT	BFT46	S7/S5	Mm/FET	BGX25	S2a	ThM
BFQ63	S10	WBT	BFT92;R	S7	Mm	BGY22	S6	RFP
BFQ65	S10	WBT	BFT93;R	S7	Mm	BGY22A	S6	RFP
BFQ66	S10	WBT	BFW10	S5	FET	BGY23	S6	RFP
BFQ68	S10	WBT	BFW11	S5	FET	BGY23A	S6	RFP
BFQ136	S10	WBT	BFW12	S5	FET	BGY32	S6	RFP
BFR29	S5	FET	BFW13	S5	FET	BGY33	S6	RFP
BFR30	S7/S5	Mm/FET	BFW16A	S10	WBT	BGY35	S6	RFP
BFR31	S7/S5	Mm/FET	BFW17A	S10	WBT	BGY36	S6	RFP
BFR49	S10	WBT	BFW30	S10	WBT	BGY40A	S6	RFP
BFR53;R	S7	Mm	BFW61	S5	FET	BGY40B	S6	RFP
BFR54	S3	Sm	BFW92	S10	WBT	BGY41A	S6	RFP
BFR64	S10	WBT	BFW92A	S10	WBT	BGY41B	S6	RFP
BFR65	S10	WBT	BFW93	S10	WBT	BGY43	S6	RFP
BFR84	S5	FET	BFX29	S3	Sm	BGY45A	S6	RFP
BFR90	S10	WBT	BFX30	S3	Sm	BGY45B	S6	RFP
BFR90A	S10	WBT	BFX34	S3	Sm	BGY46A	S6	RFP
BFR91	S10	WBT	BFX84	S3	Sm	BGY46B	S6	RFP
BFR91A	S10	WBT	BFX85	S3	Sm	BGY47*	S6	RFP
BFR92;R	S7	Mm	BFX86	S3	Sm	BGY50	S10	WBM
BFR92A;R	S7	Mm	BFX87	S3	Sm	BGY51	S10	WBM
BFR93;R	S7	Mm	BFX88	S3	Sm	BGY52	S10	WBM
BFR93A;R	S7	Mm	BFX89	S10	WBT	BGY53	S10	WBM
BFR94	S10	WBT	BFY50	S3	Sm	BGY54	S10	WBM
BFR95	S10	WBT	BFY51	S3	Sm	BGY55	S10	WBM
BFR96	S10	WBT	BFY52	S3	Sm	BGY56	S10	WBM
BFR96S	S10	WBT	BFY55	S3	Sm	BGY57	S10	WBM
BFR101A;B	S7/S5	Mm/FET	BFY90	S10	WBT	BGY58	S10	WBM
BFS17;R	S7	Mm	BG2000	S1	RT	BGY58A	S10	WBM

\* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors  
for hybrid circuits

RFP = R.F. power transistors and modules

RT = Tripler

Sm = Small-signal transistors

ThM = Thyristor modules

WBM = Wideband hybrid IC modules

WBT = Wideband hybrid IC transistors

type no.	book	section	type no.	book	section	type no.	book	section
BGY59	S10	WBM	BLV37	S6	RFP	BLW96	S6	RFP
BGY60	S10	WBM	BLV45/12	S6	RFP	BLW97	S6	RFP
BGY61	S10	WBM	BLV57	S6	RFP	BLW98	S6	RFP
BGY65	S10	WBM	BLV59	S6	RFP	BLW99	S6	RFP
BGY67	S10	WBM	BLV75/12	S6	RFP	BLX13	S6	RFP
BGY67A	S10	WBM	BLV80/28	S6	RFP	BLX13C	S6	RFP
BGY70	S10	WBM	BLV90	S6	RFP	BLX14	S6	RFP
BGY71	S10	WBM	BLV91	S6	RFP	BLX15	S6	RFP
BGY74	S10	WBM	BLV92	S6	RFP	BLX39	S6	RFP
BGY75	S10	WBM	BLV93	S6	RFP	BLX65	S6	RFP
BGY84	S10	WBM	BLV94	S6	RFP	BLX65E	S6	RFP
BGY84A	S10	WBM	BLV95	S6	RFP	BLX67	S6	RFP
BGY85	S10	WBM	BLV96	S6	RFP	BLX68	S6	RFP
BGY85A	S10	WBM	BLV97	S6	RFP	BLX69A	S6	RFP
BGY93A	S6	RFP	BLV98	S6	RFP	BLX91A	S6	RFP
BGY93B	S6	RFP	BLV99	S6	RFP	BLX91CB	S6	RFP
BGY93C	S6	RFP	BLW29	S6	RFP	BLX92A	S6	RFP
BLU20/12	S6	RFP	BLW31	S6	RFP	BLX93A	S6	RFP
BLU30/12	S6	RFP	BLW32	S6	RFP	BLX94A	S6	RFP
BLU45/12	S6	RFP	BLW33	S6	RFP	BLX94C	S6	RFP
BLU50	S6	RFP	BLW34	S6	RFP	BLX95	S6	RFP
BLU51	S6	RFP	BLW50F	S6	RFP	BLX96	S6	RFP
BLU52	S6	RFP	BLW60	S6	RFP	BLX97	S6	RFP
BLU53	S6	RFP	BLW60C	S6	RFP	BLX98	S6	RFP
BLU60/12	S6	RFP	BLW76	S6	RFP	BLY85	S6	RFP
BLU97	S6	RFP	BLW77	S6	RFP	BLY87A	S6	RFP
BLU98	S6	RFP	BLW78	S6	RFP	BLY87C	S6	RFP
BLU99	S6	RFP	BLW79	S6	RFP	BLY88A	S6	RFP
BLV10	S6	RFP	BLW80	S6	RFP	BLY88C	S6	RFP
BLV11	S6	RFP	BLW81	S6	RFP	BLY89A	S6	RFP
BLV20	S6	RFP	BLW82	S6	RFP	BLY89C	S6	RFP
BLV21	S6	RFP	BLW83	S6	RFP	BLY90	S6	RFP
BLV25	S6	RFP	BLW84	S6	RFP	BLY91A	S6	RFP
BLV30	S6	RFP	BLW85	S6	RFP	BLY91C	S6	RFP
BLV30/12	S6	RFP	BLW86	S6	RFP	BLY92A	S6	RFP
BLV31	S6	RFP	BLW87	S6	RFP	BLY92C	S6	RFP
BLV32F	S6	RFP	BLW89	S6	RFP	BLY93A	S6	RFP
BLV33	S6	RFP	BLW90	S6	RFP	BLY93C	S6	RFP
BLV33F	S6	RFP	BLW91	S6	RFP	BLY94	S6	RFP
BLV36	S6	RFP	BLW95	S6	RFP	BLY97	S6	RFP

RFP = R.F. power transistors and modules

WBM = Wideband hybrid IC modules

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type no.	book	section	type no.	book	section	type no.	book	section
BPF10	S8	PDT	BSR33	S7	Mm	BST80	S5	FET
BPF24	S8	PDT	BSR40	S7	Mm	BST82	S5	FET
BPW22A	S8	PDT	BSR41	S7	Mm	BST84	S5	FET
BPW50	S8	PDT	BSR42	S7	Mm	BST86	S5	FET
BPX25	S8	PDT	BSR43	S7	Mm	BST90	S5	FET
BPX29	S8	PDT	BSR50	S3	Sm	BST97	S5	FET
BPX40	S8	PDT	BSR51	S3	Sm	BST100	S5	FET
BPX41	S8	PDT	BSR52	S3	Sm	BST110	S5	FET
BPX42	S8	PDT	BSR56	S7/S5	Mm/FET	BST120	S5	FET
BPX71	S8	PDT	BSR57	S7/S5	Mm/FET	BST122	S5	FET
BPX72	S8	PDT	BSR58	S7/S5	Mm/FET	BSV15	S3	Sm
BPX95C	S8	PDT	BSR60	S3	Sm	BSV16	S3	Sm
BR100/03	S2b	Th	BSR61	S3	Sm	BSV17	S3	Sm
BR101	S3	Sm	BSR62	S3	Sm	BSV52;R	S7	Mm
BRY39	S3	Sm	BSS38	S3	Sm	BSV64	S3	Sm
BRY56	S3	Sm	BSS50	S3	Sm	BSV78	S5	FET
BRY61	S7	Mm	BSS51	S3	Sm	BSV79	S5	FET
BRY62	S7	Mm	BSS52	S3	Sm	BSV80	S5	FET
BS107	S5	FET	BSS60	S3	Sm	BSV81	S5	FET
BS170	S5	FET	BSS61	S3	Sm	BSW66A	S3	Sm
BSD10	S5	FET	BSS62	S3	Sm	BSW67A	S3	Sm
BSD12	S5	FET	BSS63;R	S7	Mm	BSW68A	S3	Sm
BSD20	S5/7	FET	BSS64;R	S7	Mm	BSX19	S3	Sm
BSD22	S5/7	FET	BSS68	S3	Sm	BSX20	S3	Sm
BSD212	S5	FET	BSS83	S5/7	FET/Mm	BSX45	S3	Sm
BSD213	S5	FET	BST15	S7	Mm	BSX46	S3	Sm
BSD214	S5	FET	BST16	S7	Mm	BSX47	S3	Sm
BSD215	S5	FET	BST39	S7	Mm	BSX59	S3	Sm
BSR12;R	S7	Mm	BST40	S7	Mm	BSX60	S3	Sm
BSR13;R	S7	Mm	BST50	S7	Mm	BSX61	S3	Sm
BSR14;R	S7	Mm	BST51	S7	Mm	BSY95A	S3	Sm
BSR15;R	S7	Mm	BST52	S7	Mm	BT136*	S2b	Tri
BSR16;R	S7	Mm	BST60	S7	Mm	BT137*	S2b	Tri
BSR17;R	S7	Mm	BST61	S7	Mm	BT138*	S2b	Tri
BSR17A;R	S7	Mm	BST62	S7	Mm	BT139*	S2b	Tri
BSR18;R	S7	Mm	BST70A	S5	FET	BT149*	S2b	Th
BSR18A;R	S7	Mm	BST72A	S5	FET	BT151*	S2b	Th
BSR30	S7	Mm	BST74A	S5	FET	BT152*	S2b	Th
BSR31	S7	Mm	BST76A	S5	FET	BT153	S2b	Th
BSR32	S7	Mm	BST78	S5	FET	BT155*	S2b	Th

\* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors  
for hybrid circuits

Sm = Small-signal transistors

PDT = Photodiodes or transistors

Th = Thyristors

Tri = Triacs



type no.	book	section	type no.	book	section	type no.	book	section
BT157*	S2b	Th	BUV83	S4b	SP	BUZ36	S9	PM
BTV24*	S2b	Th	BUV89	S4b	SP	BUZ40	S9	PM
BTV34*	S2b	Tri	BUW11;A	S4b	SP	BUZ41A	S9	PM
BTV58*	S2b	Th	BUW12;A	S4b	SP	BUZ42	S9	PM
BTV59*	S2b	Th	BUW13;A	S4b	SP	BUZ43	S9	PM
BTW60*	S2b	Th	BUW84	S4b	SP	BUZ44A	S9	PM
BTW23*	S2b	Th	BUW85	S4b	SP	BUZ45	S9	PM
BTW38*	S2b	Th	BUX46;A	S4b	SP	BUZ45A	S9	PM
BTW40*	S2b	Th	BUX47;A	S4b	SP	BUZ45B	S9	PM
BTW42*	S2b	Th	BUX48;A	S4b	SP	BUZ45C	S9	PM
BTW43*	S2b	Tri	BUX80	S4b	SP	BUZ46	S9	PM
BTW45*	S2b	Th	BUX81	S4b	SP	BUZ50A	S9	PM
BTW58*	S2b	Th	BUX82	S4b	SP	BUZ50B	S9	PM
BTW59*	S2b	Th	BUX83	S4b	SP	BUZ53A	S9	PM
BTW63*	S2b	Th	BUX84	S4b	SP	BUZ54	S9	PM
BTW92*	S2b	Th	BUX85	S4b	SP	BUZ54A	S9	PM
BTX18*	S2b	Th	BUX86	S4b	SP	BUZ60	S9	PM
BTX94*	S2b	Tri	BUX87	S4b	SP	BUZ60B	S9	PM
BTY79*	S2b	Th	BUX88	S4b	SP	BUZ63	S9	PM
BTY91*	S2b	Th	BUX90	S4b	SP	BUZ63B	S9	PM
BU208A	S4b	SP	BUX98	S4b	SP	BUZ64	S9	PM
BU208B	S4b	SP	BUX98A	S4b	SP	BUZ71	S9	PM
BU326	S4b	SP	BUY89	S4b	SP	BUZ71A	S9	PM
BU326A	S4b	SP	BUZ10	S9	PM	BUZ72	S9	PM
BU426	S4b	SP	BUZ10A	S9	PM	BUZ72A	S9	PM
BU426A	S4b	SP	BUZ11	S9	PM	BUZ73A	S9	PM
BU433	S4b	SP	BUZ11A	S9	PM	BUZ74	S9	PM
BU505	S4b	SP	BUZ14	S9	PM	BUZ74A	S9	PM
BU508A	S4b	SP	BUZ15	S9	PM	BUZ76	S9	PM
BU705	S4b	SP	BUZ20	S9	PM	BUZ76A	S9	PM
BU806	S4b	SP	BUZ21	S9	PM	BUZ80	S9	PM
BU807	S4b	SP	BUZ23	S9	PM	BUZ80A	S9	PM
BU824	S4b	SP	BUZ24	S9	PM	BUZ83	S9	PM
BU826	S4b	SP	BUZ25	S9	PM	BUZ83A	S9	PM
BUS11;A	S4b	SP	BUZ30	S9	PM	BUZ84	S9	PM
BUS12;A	S4b	SP	BUZ31	S9	PM	BUZ84A	S9	PM
BUS13;A	S4b	SP	BUZ32	S9	PM	BY228	S1	R
BUS14;A	S4b	SP	BUZ33	S9	PM	BY229*	S2a	R
BUT11;A	S4b	SP	BUZ34	S9	PM	BY249*	S2a	R
BUV82	S4b	SP	BUZ35	S9	PM	BY260*	S2a	R

\* = series

PM = Power MOS transistors

R = Rectifier diodes

SP = Low-frequency switching power transistors

Th = Thyristors

Tri = Triacs

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type no.	book	section	type no.	book	section	type no.	book	section
BY261*	S2a	R	BYV28*	S1/S2a	R	BYX46*	S2a	R
BY329*	S2a	R	BYV29*	S2a	R	BYX50*	S2a	R
BY359*	S2a	R	BYV30*	S2a	R	BYX52*	S2a	R
BY438	S1	R	BYV32*	S2a	R	BYX56*	S2a	R
BY448	S1	R	BYV33*	S2a	R	BYX90G	S1	R
BY458	S1	R	BYV34*	S2a	R	BYX94	S1	R
BY505	S1	R	BYV36*	S1	R	BYX96*	S2a	R
BY509	S1	R	BYV39*	S2a	R	BYX97*	S2a	R
BY527	S1	R	BYV42*	S2a	R	BYX98*	S2a	R
BY584	S1	R	BYV43*	S2a	R	BYX99*	S2a	R
BY588	S1	R	BYV72*	S2a	R	BZD23	S1	Vrg
BY609	S1	R	BYV73*	S2a	R	BZT03	S1	Vrg
BY610	S1	R	BYV79*	S2a	R	BZV10	S1	Vrf
BY614	S1	R	BYV92*	S2a	R	BZV11	S1	Vrf
BY619	S1	R	BYV95A	S1	R	BZV12	S1	Vrf
BY620	S1	R	BYV95B	S1	R	BZV13	S1	Vrf
BY707	S1	R	BYV95C	S1	R	BZV14	S1	Vrf
BY708	S1	R	BYV96D	S1	R	BZV37	S1	Vrf
BY709	S1	R	BYV96E	S1	R	BZV46	S1	Vrg
BY710	S1	R	BYW25*	S2a	R	BZV49*	S1/S7	Vrg/Mm
BY711	S1	R	BYW29*	S2a	R	BZV55*	S7	Mm
BY712	S1	R	BYW30*	S2a	R	BZV85*	S1	Vrg
BY713	S1	R	BYW31*	S2a	R	BZW03*	S1	Vrg
BY714	S1	R	BYW54	S1	R	BZW14	S1	Vrg
BYD13*	S1	R	BYW55	S1	R	BZW70*	S2a	TS
BYD33*	S1	R	BYW56	S1	R	BZW86*	S2a	TS
BYD73*	S1	R	BYW92*	S2a	R	BZW91*	S2a	TS
BYM56*	S1	R	BYW93*	S2a	R	BZX55*	S1	Vrg
BYQ28*	S2a	R	BYW94*	S2a	R	BZX70*	S2a	Vrg
BYR29*	S2a	R	BYW95A	S1	R	BZX75*	S1	Vrg
BYT79*	S2a	R	BYW95B	S1	R	BZX79*	S1	Vrg
BYV10	S1	R	BYW95C	S1	R	BZX84*	S7/S1	Mm/Vrg
BYV19*	S2a	R	BYW96D	S1	R	BZX90	S1	Vrf
BYV20*	S2a	R	BYW96E	S1	R	BZX91	S1	Vrf
BYV21*	S2a	R	BYX25*	S2a	R	BZX92	S1	Vrf
BYV22*	S2a	R	BYX30*	S2a	R	BZX93	S1	Vrf
BYV23*	S2a	R	BYX32*	S2a	R	BZX94	S1	Vrf
BYV24*	S2a	R	BYX38*	S2a	R	BZY91*	S2a	Vrg
BYV26*	S1	R	BYX39*	S2a	R	BZY93*	S2a	Vrg
BYV27*	S1/S2a	R	BYX42*	S2a	R	BZY95*	S2a	Vrg

\* = series

Mm = Microminiature semiconductors  
for hybrid circuits

R = Rectifier diodes

TS = Transient suppressor diodes

Vrf = Voltage reference diodes

Vrg = Voltage regulator diodes

type no.	book	section	type no.	book	section	type no.	book	section
BZY96*	S2a	Vrg	CQV61A(L)	S8	LED	CQY89A	S8	LED
CNX21	S8	PhC	CQV62(L)	S8	LED	CQY94	S8	LED
CNX35	S8	PhC	CQV70(L)	S8	LED	CQY94B(L)	S8	LED
CNX36	S8	PhC	CQV70A(L)	S8	LED	CQY95B	S8	LED
CNX37	S8	PhC	CQV71A(L)	S8	LED	CQY96(L)	S8	LED
CNX38	S8	PhC	CQV72(L)	S8	LED	CQY97A	S8	LED
CNX44	S8	PhC	CQV80L	S8	LED	OM320	S10	WBM
CNX48	S8	PhC	CQV80AL	S8	LED	OM321	S10	WBM
CNX62	S8	PhC	CQV81L	S8	LED	OM322	S10	WBM
CNY50	S8	PhC	CQV82L	S8	LED	OM323	S10	WBM
CNY52	S8	PhC	CQW10(L)	S8	LED	OM323A	S10	WBM
CNY53	S8	PhC	CQW10A(L)	S8	LED	OM335	S10	WBM
CNY57	S8	PhC	CQW10B(L)	S8	LED	OM336	S10	WBM
CNY57A	S8	PhC	CQW11A(L)	S8	LED	OM337	S10	WBM
CNY62	S8	PhC	CQW11B(L)	S8	LED	OM337A	S10	WBM
CNY63	S8	PhC	CQW12(L)	S8	LED	OM339	S10	WBM
CQ209S	S8	D	CQW12B(L)	S8	LED	OM345	S10	WBM
CQ216X	S8	D	CQW20A	S8	LED	OM350	S10	WBM
CQ216Y	S8	D	CQW21	S8	LED	OM360	S10	WBM
CQ327;R	S8	D	CQW22	S8	LED	OM361	S10	WBM
CQ330;R	S8	D	CQW24(L)	S8	LED	OM370	S10	WBM
CQ331;R	S8	D	CQW54	S8	LED	OM931	S4a	P
CQ332;R	S8	D	CQX10	S8	LED	OM961	S4a	P
CQ427;R	S8	D	CQX11	S8	LED	OSB9110	S2a	St
CQ430;R	S8	D	CQX12	S8	LED	OSB9115	S2a	St
CQ431;R	S8	D	CQX24(L)	S8	LED	OSB9210	S2a	St
CQ432;R	S8	D	CQX51	S8	LED	OSB9215	S2a	St
CQF24	S8	Ph	CQX54(L)	S8	LED	OSB9410	S2a	St
CQL10A	S8	Ph	CQX64(L)	S8	LED	OSB9415	S2a	St
CQL13	S8	Ph	CQX74(L)	S8	LED	OSM9110	S2a	St
CQL13A	S8	Ph	CQX74Y	S8	LED	OSM9115	S2a	St
CQL14A	S8	Ph	CQY11B	S8	LED	OSM9210	S2a	St
CQL14B	S8	Ph	CQY11C	S8	LED	OSM9215	S2a	St
CQN10	S8	LED	CQY24B(L)	S8	LED	OSM9410	S2a	St
CQN11	S8	LED	CQY49B	S8	LED	OSM9415	S2a	St
CQT10	S8	LED	CQY49C	S8	LED	OSM9510	S2a	St
CQT11	S8	LED	CQY50	S8	LED	OSM9511	S2a	St
CQT12	S8	LED	CQY52	S8	LED	OSM9512	S2a	St
CQV60(L)	S8	LED	CQY54A	S8	LED	OSS9110	S2a	St
CQV60A(L)	S8	LED	CQY58A	S8	LED	OSS9115	S2a	St

\* = series  
 D = Displays  
 LED = Light-emitting diodes  
 P = Low-frequency power transistors  
 Ph = Photoconductive devices

PhC = Photocouplers  
 St = Rectifier stacks  
 WBM = Wideband hybrid IC modules  
 Vrg = Voltage regulator diodes

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type no.	book	section	type no.	book	section	type no.	book	section
OSS9210	S2a	St	1N3882	S2a	R	2N1711	S3	Sm
OSS9215	S2a	St	1N3883	S2a	R	2N1893	S3	Sm
OSS9410	S2a	St	1N3889	S2a	R	2N2219	S3	Sm
OSS9415	S2a	St	1N3890	S2a	R	2N2219A	S3	Sm
PBMF4391	S5	FET	1N3891	S2a	R	2N2222	S3	Sm
PBMF4392	S5	FET	1N3892	S2a	R	2N2222A	S3	Sm
PBMF4393	S5	FET	1N3893	S2a	R	2N2297	S3	Sm
PH2222;R	S3	Sm	1N3909	S2a	R	2N2368	S3	Sm
PH2222A;R	S3	Sm	1N3910	S2a	R	2N2369	S3	Sm
PH2369	S3	Sm	1N3911	S2a	R	2N2369A	S3	Sm
PH2907;R	S3	Sm	1N3912	S2a	R	2N2483	S3	Sm
PH2907A;R	S3	Sm	1N3913	S2a	R	2N2484	S3	Sm
PH2955T	S4a	P	1N4001G	S1	R	2N2904	S3	Sm
PH3055T	S4a	P	1N4002G	S1	R	2N2904A	S3	Sm
PH5415	S3	Sm	1N4003G	S1	R	2N2905	S3	Sm
PH5416	S3	Sm	1N4004G	S1	R	2N2905A	S3	Sm
PHSD51	S2a	R	1N4005G	S1	R	2N2906	S3	Sm
RPY58A	S8	Ph	1N4006G	S1	R	2N2906A	S3	Sm
RPY76B	S8	Ph	1N4007G	S1	R	2N2907	S3	Sm
RPY86	S8	I	1N4148	S1	SD	2N2907A	S3	Sm
RPY87	S8	I	1N4150	S1	SD	2N3019	S3	Sm
RPY88	S8	I	1N4151	S1	SD	2N3020	S3	Sm
RPY89	S8	I	1N4153	S1	SD	2N3053	S3	Sm
RPY90*	S8	I	1N4446	S1	SD	2N3375	S6	RFP
RPY91*	S8	I	1N4448	S1	SD	2N3553	S6	RFP
RPY93	S8	I	1N4531	S1	SD	2N3632	S6	RFP
RPY94	S8	I	1N4532	S1	SD	2N3822	S5	FET
RPY95	S8	I	1N5059	S1	R	2N3823	S5	FET
RPY96	S8	I	1N5060	S1	R	2N3866	S6	RFP
RPY97	S8	I	1N5061	S1	R	2N3903	S3	Sm
1N821;A	S1	Vrf	1N5062	S1	R	2N3904	S3	Sm
1N823;A	S1	Vrf	1N5832	S2a	R	2N3905	S3	Sm
1N825;A	S1	Vrf	1N5833	S2a	R	2N3906	S3	Sm
1N827;A	S1	Vrf	1N5834	S2a	R	2N3924	S6	RFP
1N829;A	S1	Vrf	1N6097	S2a	R	2N3926	S6	RFP
1N914	S1	SD	1N6098	S2a	R	2N3927	S6	RFP
1N916	S1	SD	2N918	S10	WBT	2N3966	S5	FET
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1N3880	S2a	R	2N930	S3	Sm	2N4031	S3	Sm
1N3881	S2a	R	2N1613	S3	Sm	2N4032	S3	Sm

\* = series

FET = Field-effect transistors

I = Infrared devices

P = Low-frequency power transistors

Ph = Photoconductive devices

R = Rectifier diodes

RFP = R.F. power transistors and modules

SD = Small-signal diodes

Sm = Small-signal transistors

St = Rectifier stacks

Vrf = Voltage reference diodes

WBT = Wideband hybrid IC transistors

type no.	book	section	type no.	book	section	type no.	book	section
2N4033	S3	Sm	2N5415	S3	Sm	56352	S4b	A
2N4091	S5	FET	2N5416	S3	Sm	56353	S4b	A
2N4092	S5	FET	2N5550	S3	Sm	56354	S4b	A
2N4093	S5	FET	2N5551	S3	Sm	56359b	S2,4b	A
2N4123	S3	Sm	2N6659	S5	FET	56359c	S2,4b	A
2N4124	S3	Sm	2N6660	S5	FET	56359d	S2,4b	A
2N4125	S3	Sm	2N6661	S5	FET	56360a	S2,4b	A
2N4126	S3	Sm	61SV	S8	I	56363	S2,4b	A
2N4391	S5	FET	375CQY/B	S8	Ph	56364	S2,4b	A
2N4392	S5	FET	497CQF/A	S8	Ph	56367	S2a/b	A
2N4393	S5	FET	498CQL	S8	Ph	56368a	S2,4b	A
2N4427	S6	RFP	56201d	S4b	A	56368b	S2,4b	A
2N4856	S5	FET	56201j	S4b	A	56369	S2,4b	A
2N4857	S5	FET	56245	S3,10	A	56378	S2,4b	A
2N4858	S5	FET	56246	S3,10	A	56379	S2,4b	A
2N4859	S5	FET	56261a	S4b	A	56387a,b	S4b	A
2N4860	S5	FET	56264a,b	S2a/b	A			
2N4861	S5	FET	56295	S2a/b	A			
2N5400	S3	Sm	56326	S4b	A			
2N5401	S3	Sm	56339	S4b	A			

A = Accessories  
 FET = Field-effect transistors  
 I = Infrared devices

Ph = Photoconductive devices  
 RFP = R.F. power transistors and modules  
 Sm = Small-signal transistors

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